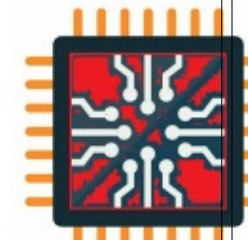


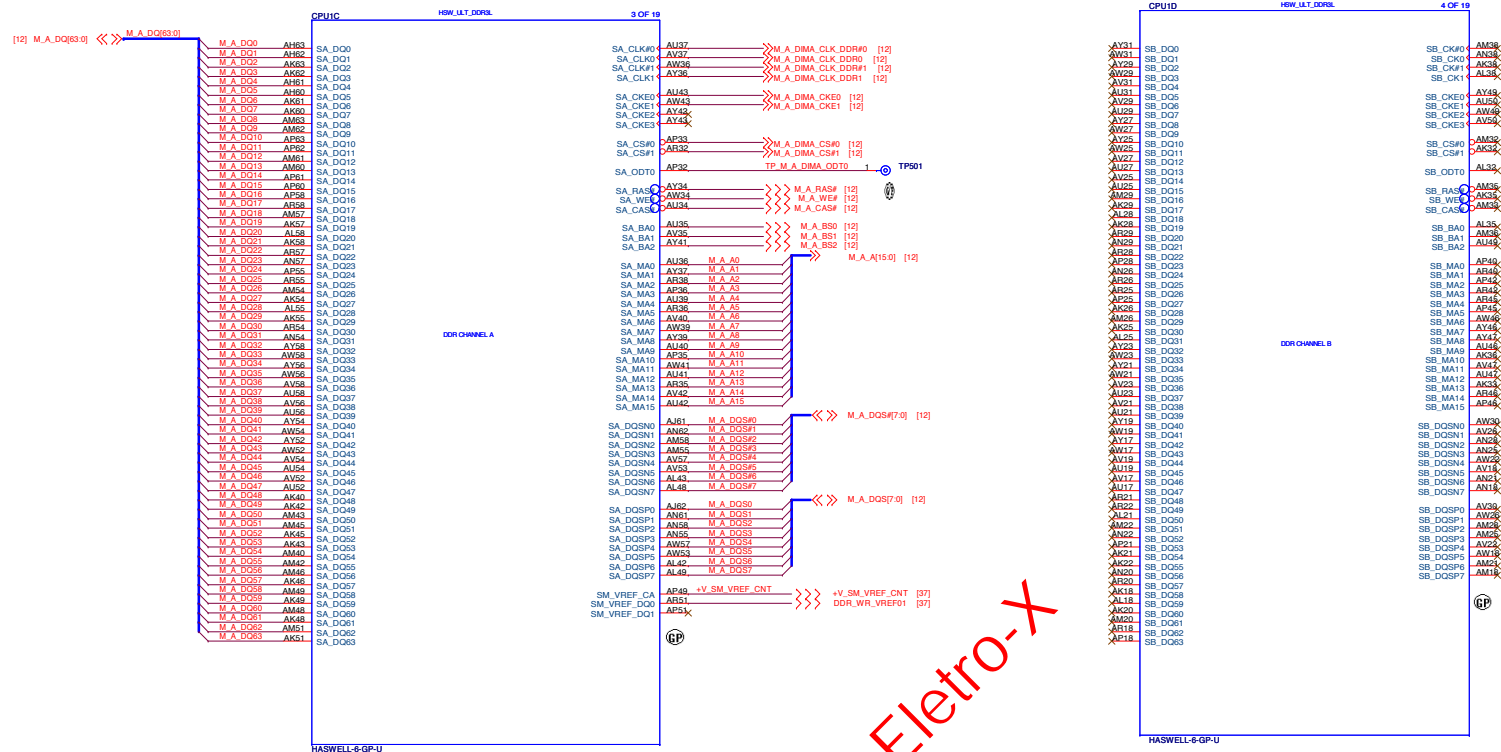
# INTEL Janus Block Diagram





**SSID = CPU**

**DDR3L ball type: Non-Interleaved Type**



Eletro-X

## Eleto-X

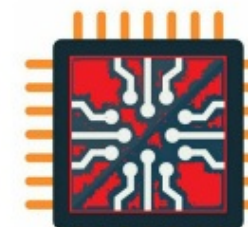
## Eleto-X

## Eleto-X

## Eleto-X

## Eleto-X

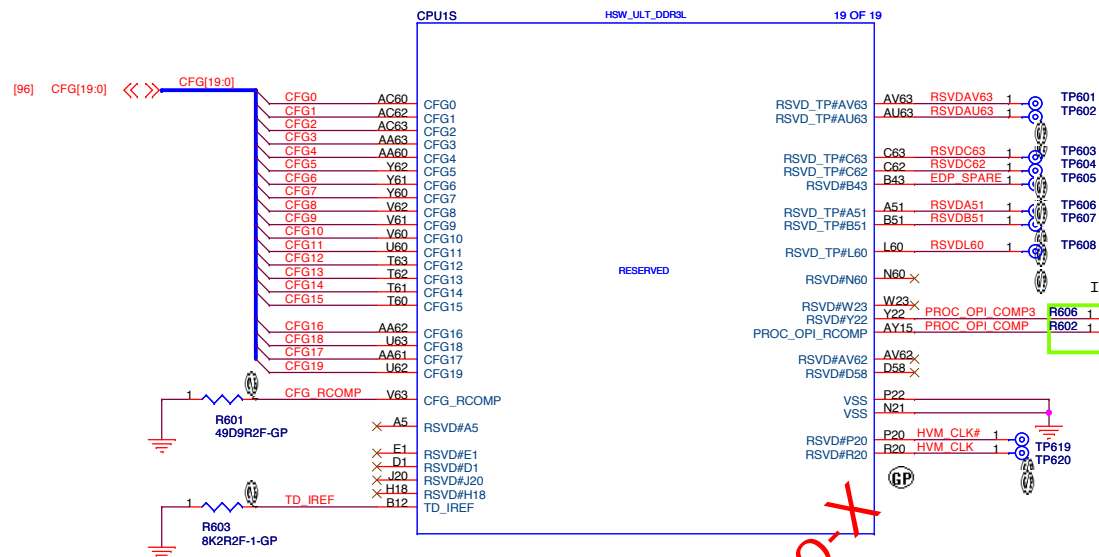
## Eleto-X



Team Electro-X

# Eleto-X

SSID = CPU



#514405

## 7.4

### Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

- RSVD - these signals should not be connected
- RSVD\_TP - these signals should be routed to a test point
- RSVD\_NCTF - these signals are non-critical to function and may be left unconnected

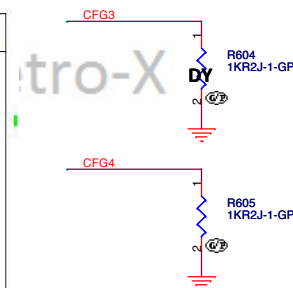
Intel Recommend

### Layout Note:

1. Referenced "continuous" VSS plane only.
2. Avoid routing next to clock pins or noisy signals.
3. Trace width: 12-15mil
4. Isolation Spacing: 12mil
5. Max length: 500mil

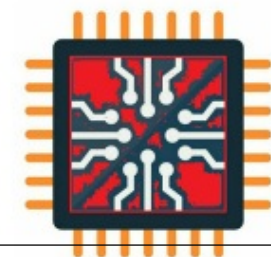
#514405 PCH strap pin:

Signal Name	Description	Direction / Buffer Type
CFG[19:0]	<p><b>Configuration Signals:</b> The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate Platform Design Guide for pull-down recommendations when a logic low is desired.</p> <ul style="list-style-type: none"><li>• <b>CFG[2:0]:</b> Reserved configuration lane. A test point may be placed on the board for these lanes.</li><li>• <b>CFG[3]: MSR Privacy Bit Feature</b><ul style="list-style-type: none"><li>— 1 = Debug capability is determined by IA32_Debug_Interface_MSR (C80h) bit[0] setting</li><li>— 0 = IA32_Debug_Interface_MSR (C80h) bit[0] default setting overridden</li></ul></li><li>• <b>CFG[4]: eDP enable</b><ul style="list-style-type: none"><li>— 1 = Disabled</li><li>— 0 = Enabled</li></ul></li><li>• <b>CFG[19:5]:</b> Reserved configuration lanes. A test point may be placed on the board for these lanes.</li></ul>	I/O GTL

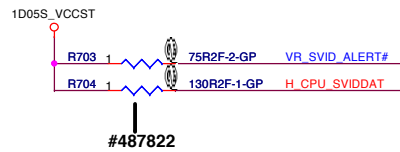


PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR 1 : DISABLED

DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT 1 : DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT

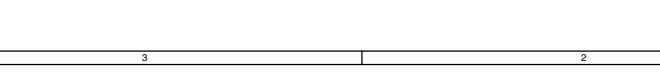
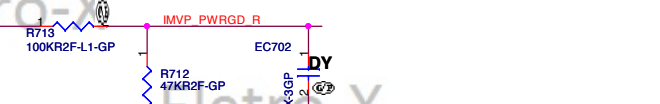
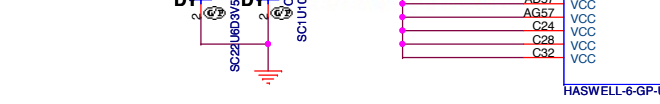
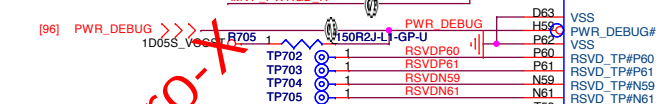
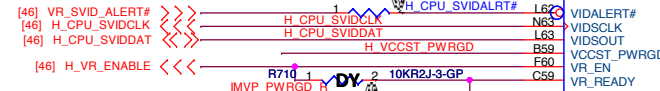
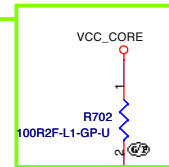


SSID = CPU

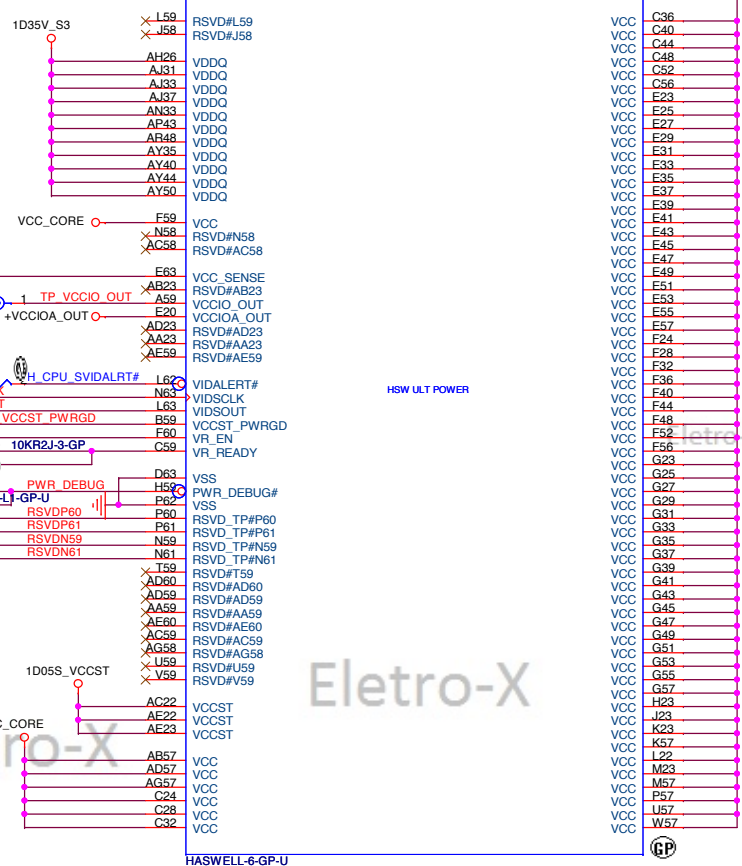


### Layout Note:

1. Place close to CPU
2. VCC\_SENSE/ VSS\_SENSE impedance=50 ohm
3. Length match<25mil



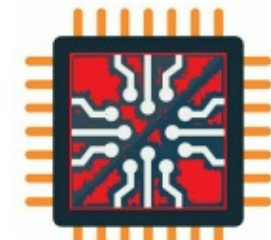
CPU1L HSW\_ULT\_DOR3L 12 OF 19 VCC\_CORE



[36,48] 1D05V\_VTT\_PWRGD >>>

Need to fine tune to 1.05v.

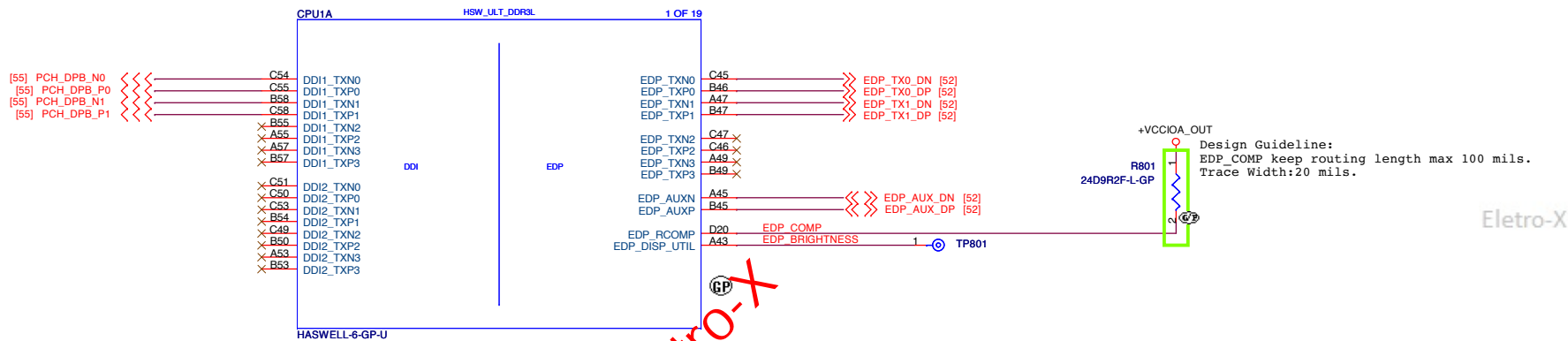
[24,46] IMVP\_PWRGD >>>



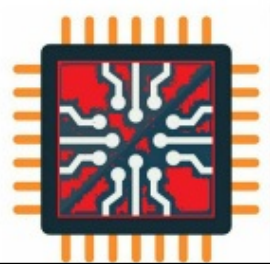
SSID = CPU

www.vinafix.vn

DP to VGA Converter

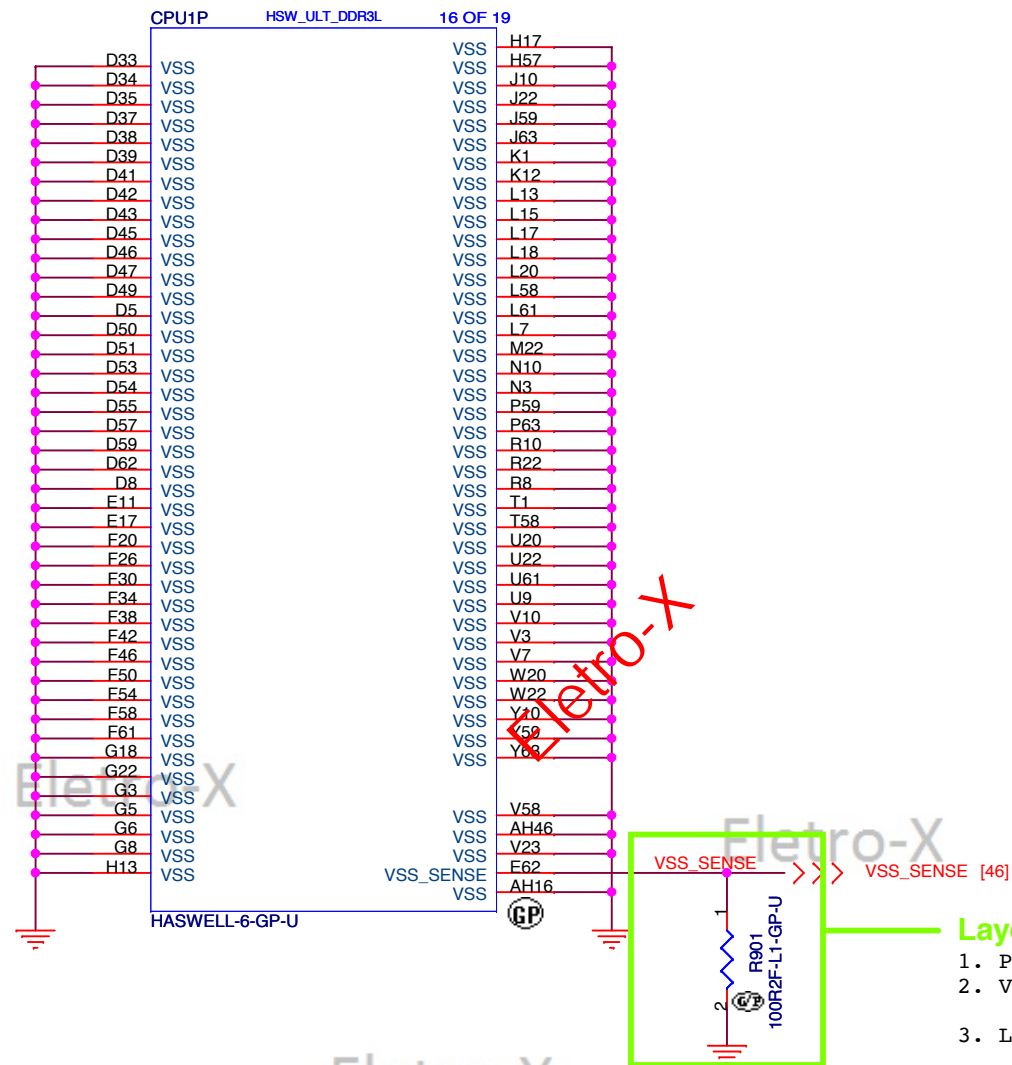


Eletro-X



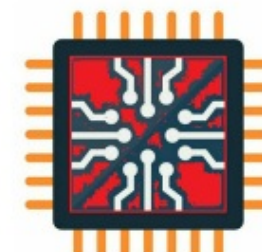
Team Eletro-X

**SSID = CPU**



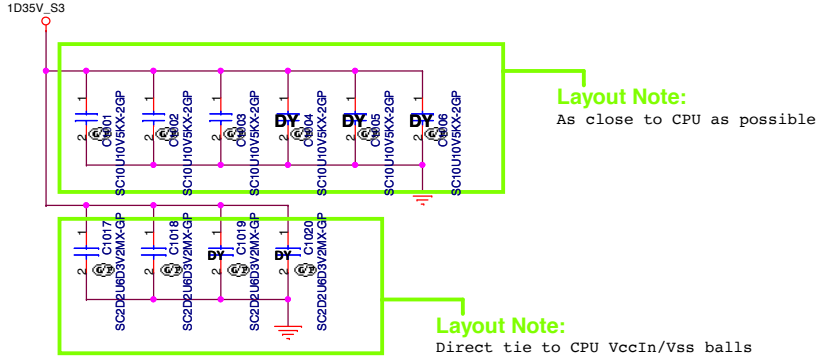
**Layout Note:**

1. Place close to CPU
2. VCC\_SENSE/ VSS\_SENSE impedance=50 ohm
3. Length match<25mil





SSID = CPU



Eletro-X

Eletro-X

Eletro-X

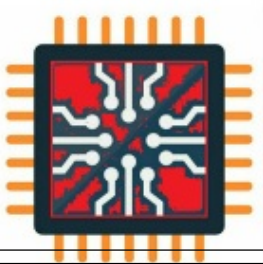
Eletro-X

Eletro-X

Eletro-X

Eletro-X

Eletro-X

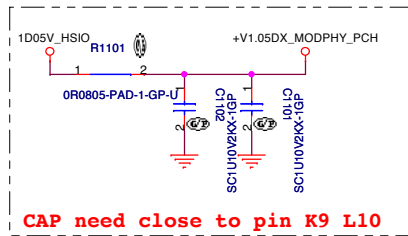


Team Eletro-X

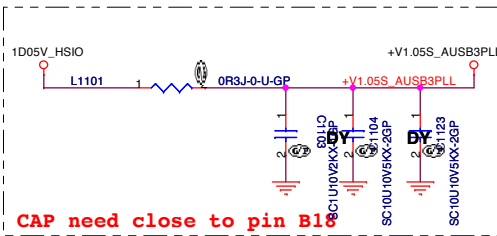


MAX: 1.92A

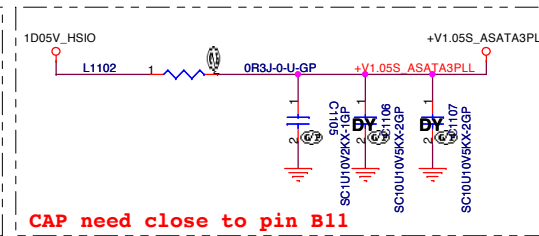
1.838A



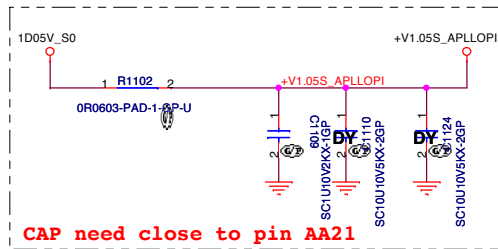
41mA



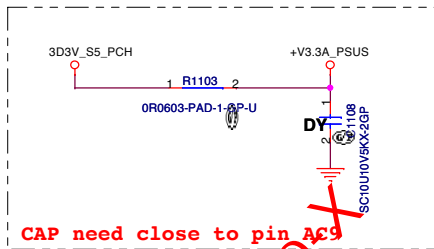
42mA



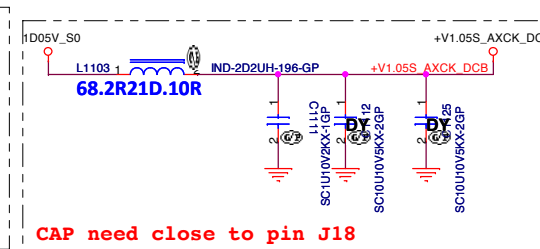
57mA



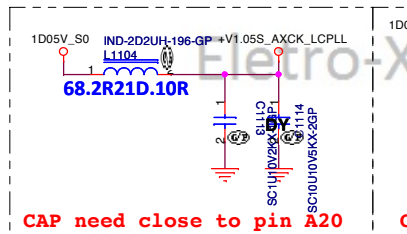
62mA



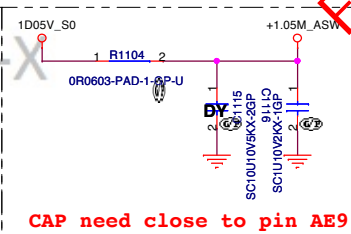
185mA



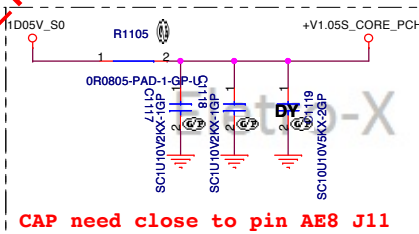
31mA



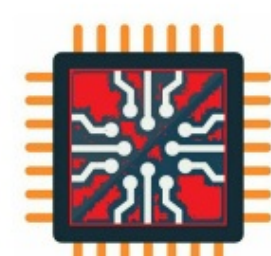
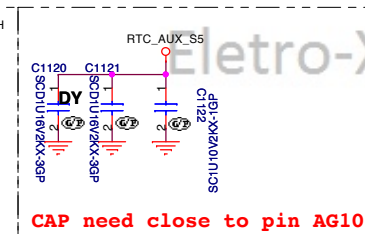
658mA



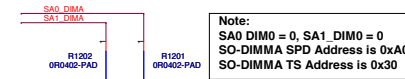
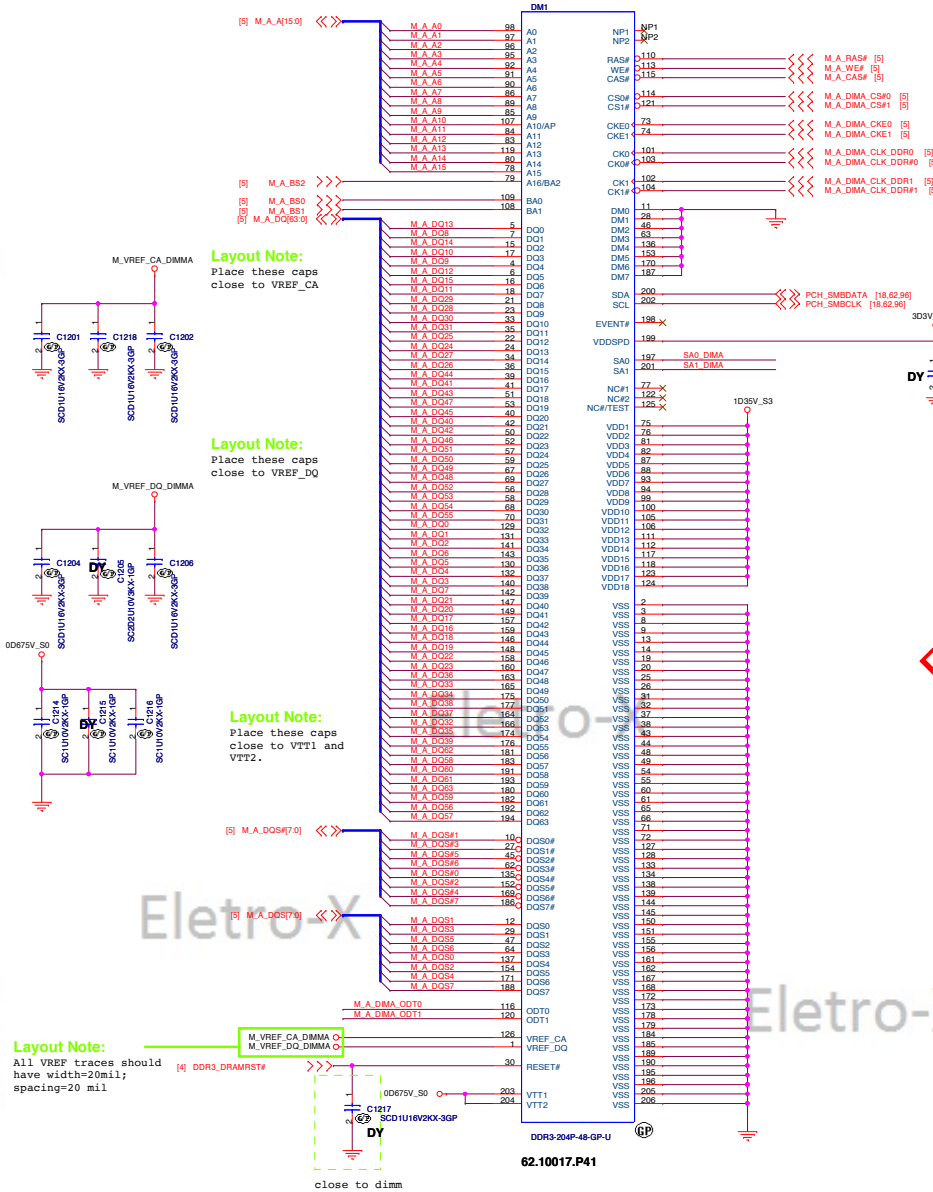
1.632A



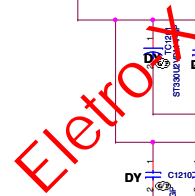
1mA



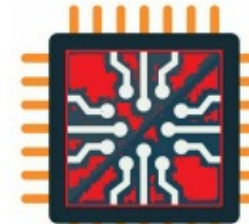
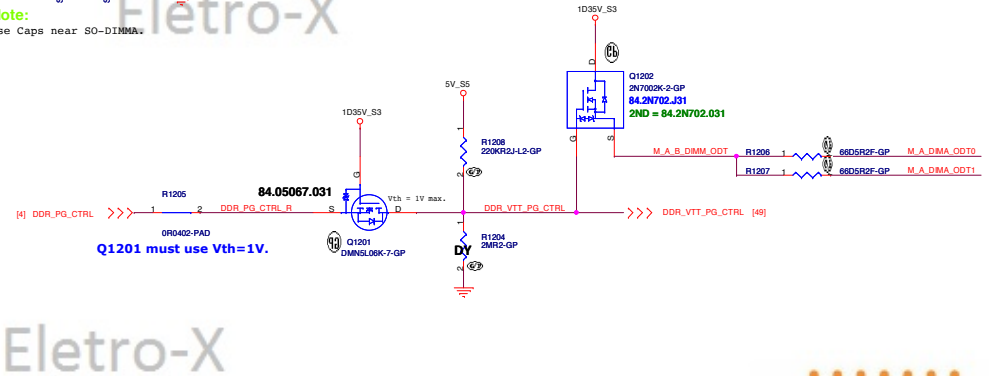
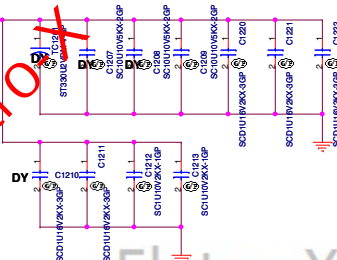
**SSID = MEMORY**



**Note:**  
SA0\_DIM0 = 0, SA1\_DIM0 = 0  
SO-DIMMA SPD Address is 0xA0  
SO-DIMMA TS Address is 0x30



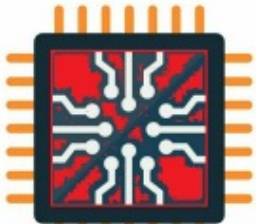
**Layout Note:**  
Place these Caps near SO-DIMM



### PCH strap pin:

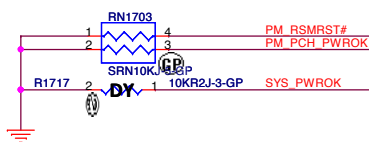
Port B Detected	
DDPB_CTRLDATA	<div> <div></div> <div>Low = Disable Port B (default) High = Enable Port B</div> </div>
DDPC_CTRLDATA	<div> <div></div> <div>Low = Disable Port C (default) High = Enable Port C</div> </div>

The internal pull-down is disabled after PLTRST# deasserts.





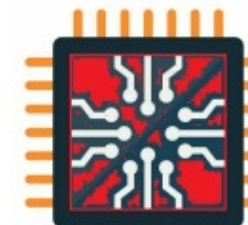
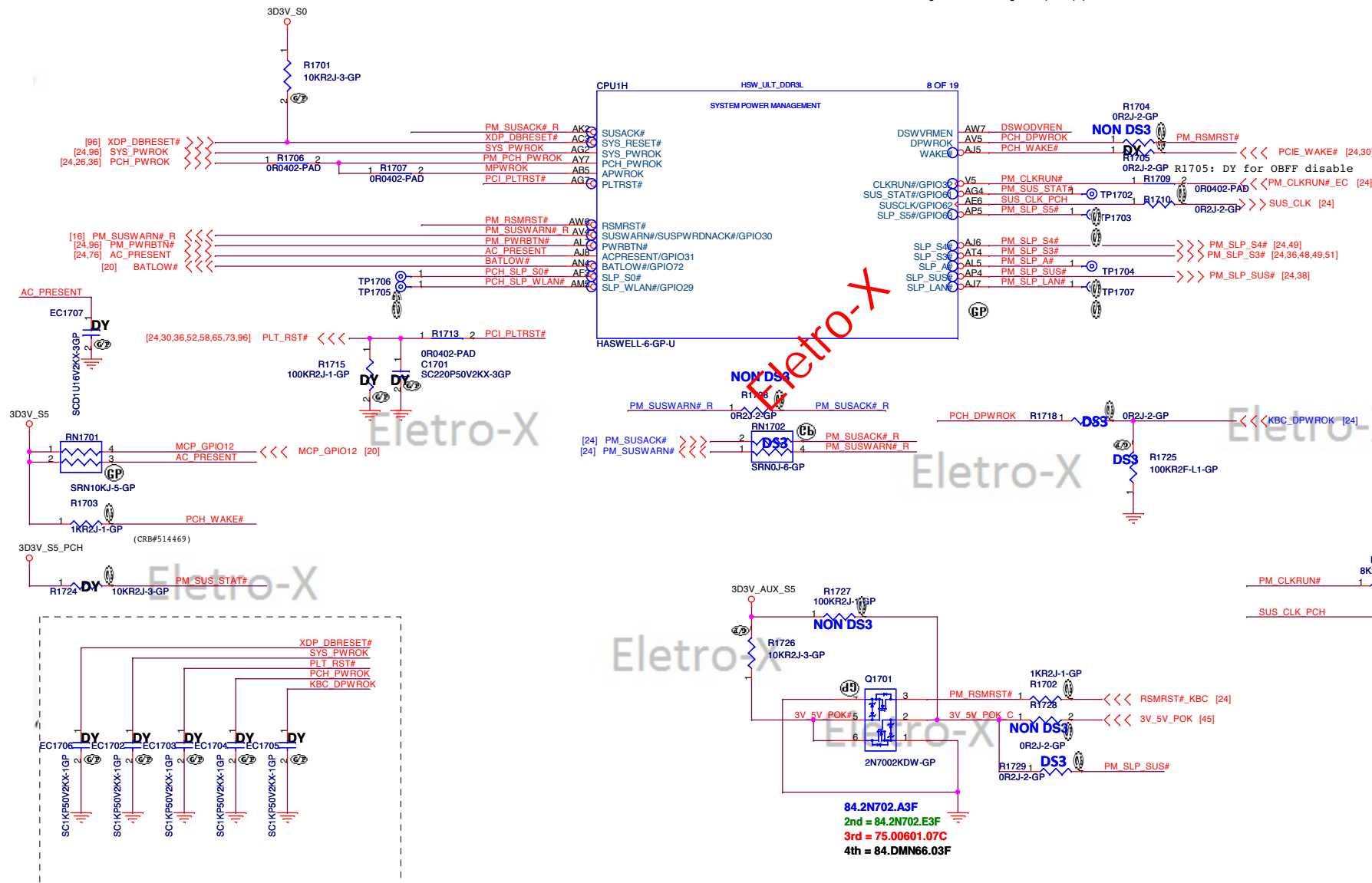
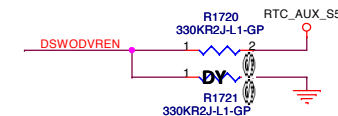
## SSID = PCH



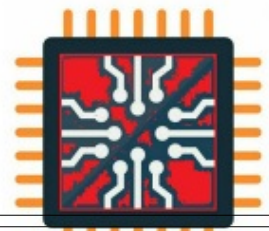
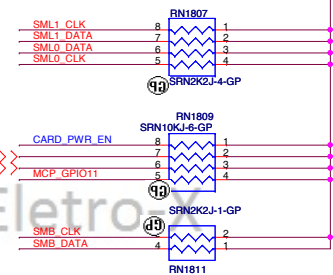
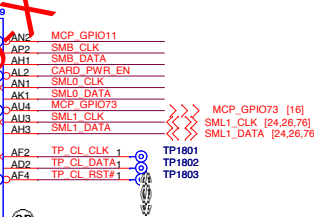
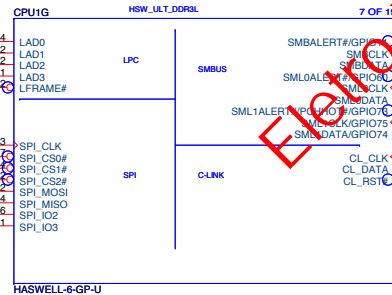
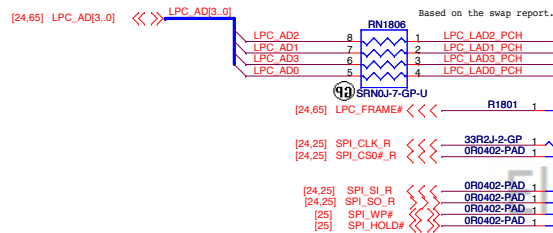
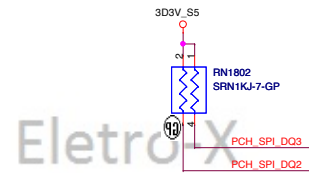
**PCH strap pin:**

On Die DSW VR Enable	
DSWVRMEN	Low = Disable * High = Enable (default)

This signal has no integrated pull-up/pull-down.



# Eleto-X

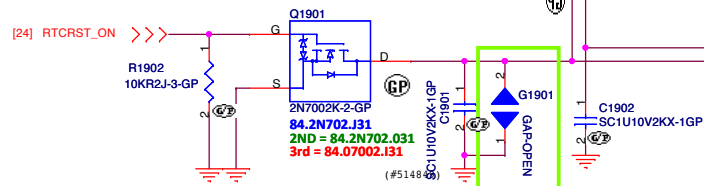
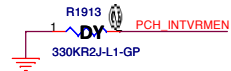




SSID = CPU

### PCH strap pin:

Integrated SUS 1V VRM Enable	
INTVRMEN	Low = External VRs High = Internal VRs*

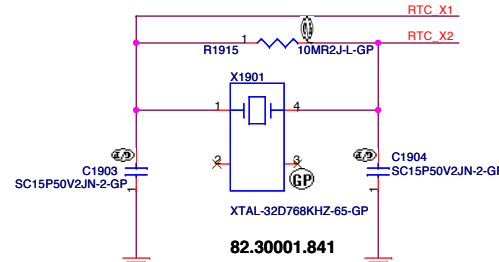
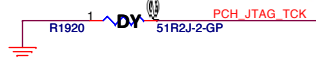
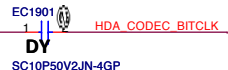
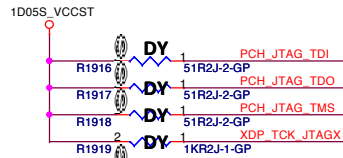


Layout: Place at the open door area.

### PCH strap pin:

Flash Descriptor Security Override/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default * High = Enable

The internal pull-down is disabled after PLTRST# deasserts



RTC X1  
RTC X2  
SM INTRUDER#  
PCH\_INTVRMEN  
SRTC\_RST#  
RTC\_RST#

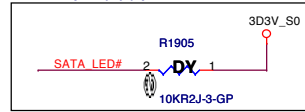
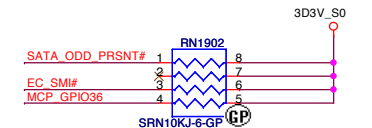
HDA\_BITCLK  
HDA\_SYNC  
HDA\_RST#  
HDA\_SDIN0  
HDA\_SDOUT  
TP\_HDA\_DOCK\_EN#

PCH\_JTAG\_TRST#  
PCH\_JTAG\_TCK  
PCH\_JTAG\_TDI  
PCH\_JTAG\_TDO  
PCH\_JTAG\_TMS  
XDP\_TCK\_JTAGX

SATA\_RN0/PERN6\_L3  
SATA\_RP0/PERP6\_L3  
SATA\_TN0/PETN6\_L3  
SATA\_TP0/PETP6\_L3  
SATA\_RN1/PERN6\_L2  
SATA\_RP1/PERP6\_L2  
SATA\_TN1/PETN6\_L2  
SATA\_TP1/PETP6\_L2  
SATA\_RN2/PERN6\_L1  
SATA\_RP2/PERP6\_L1  
SATA\_TN2/PETN6\_L1  
SATA\_TP2/PETP6\_L1  
SATA\_RN3/PERN6\_L0  
SATA\_RP3/PERP6\_L0  
SATA\_TN3/PETN6\_L0  
SATA\_TP3/PETP6\_L0

SATA0GP/GPIO34  
SATA1GP/GPIO35  
SATA2GP/GPIO36  
SATA3GP/GPIO37  
SATA\_IREF  
RSVD#L11  
RSVD#K10  
SATA\_RCOMP  
SATA\_LED#

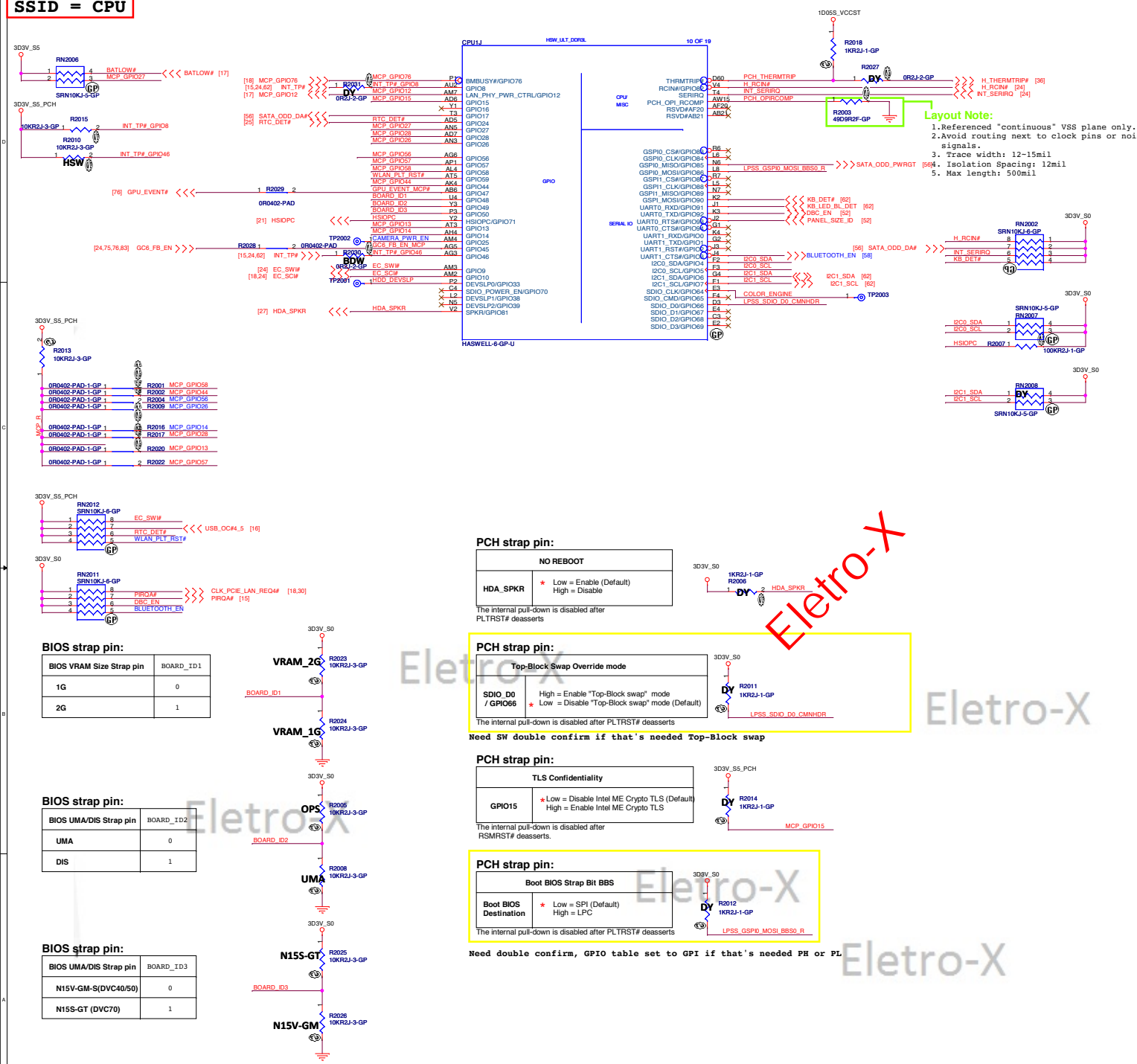
Layout Note:  
4mil trace at break-out and 3  
12-15mil trace with <0.2 ohms  
and length total <= 500mils.



Unused SATA[3:0]GP pins must be terminated to either  
3.3V rail or GND using 8.2K to 10K on the  
motherboard. Either pull-up or pull-down is acceptable.







**Layout Note:**

1. Referenced "continuous" VSS plane only.
2. Avoid routing next to clock pins or noisy signals.
3. Trace width: 12-15mil
4. Isolation Spacing: 12mil
5. Max length: 500mil

**BIOS strap pin:**

BIOS VRAM Size Strap pin	BOARD_ID1
1G	0
2G	1

**BIOS strap pin:**

BIOS UMA/DIS Strap pin	BOARD_ID2
UMA	0
DIS	1

**BIOS strap pin:**

BIOS UMA/DIS Strap pin	BOARD_ID3
N15V-GM-S(DVC40/50)	0
N15V-GT (DVC70)	1

**PCH strap pin:**

NO REBOOT	
HDA_SPKR	★ Low = Enable (Default) High = Disable

The internal pull-down is disabled after PLTRST# deasserts

**PCH strap pin:**

Top-Block Swap Override mode	
SDIO_D0 / GPIO66	★ High = Enable "Top-Block swap" mode Low = Disable "Top-Block swap" mode (Default)

The internal pull-down is disabled after PLTRST# deasserts

Need SW double confirm if that's needed Top-Block swap

**PCH strap pin:**

TLS Confidentiality	
GPIO15	★ Low = Disable Intel ME Crypto TLS (Default) High = Enable Intel ME Crypto TLS

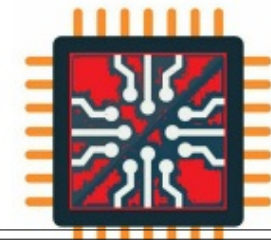
The internal pull-down is disabled after RSMRST# deasserts.

**PCH strap pin:**

Boot BIOS Strap Bit BBS	
Boot BIOS Destination	★ Low = SPI (Default) High = LPC

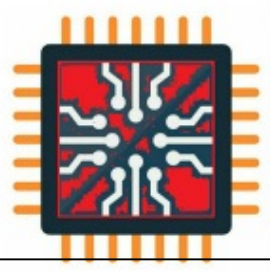
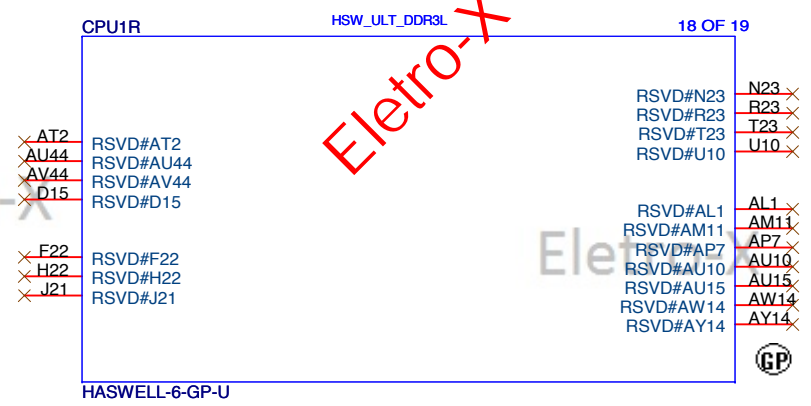
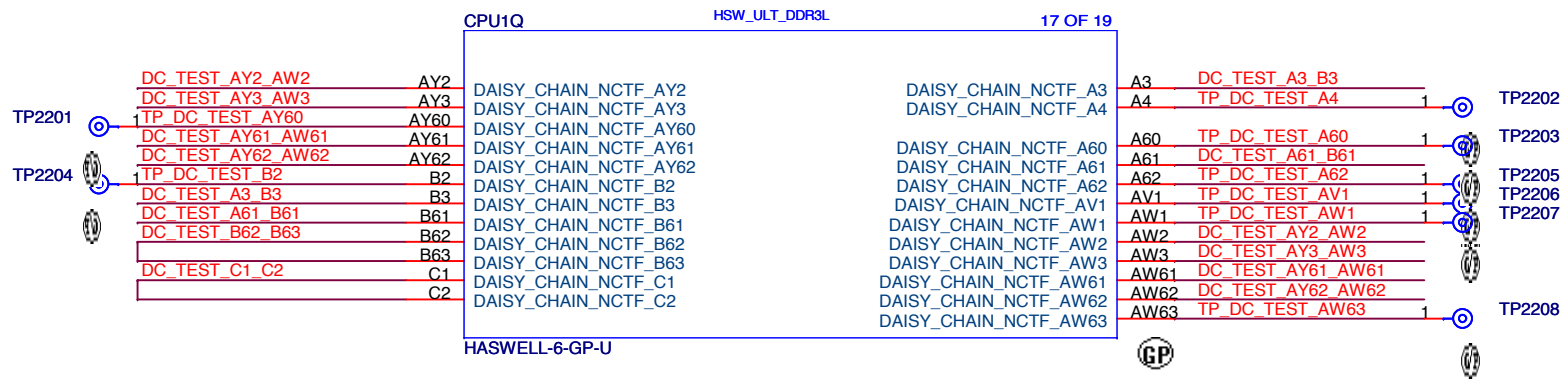
The internal pull-down is disabled after PLTRST# deasserts

Need double confirm, GPIO table set to GPI if that's needed PH or PL

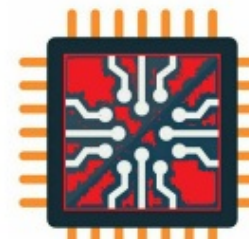
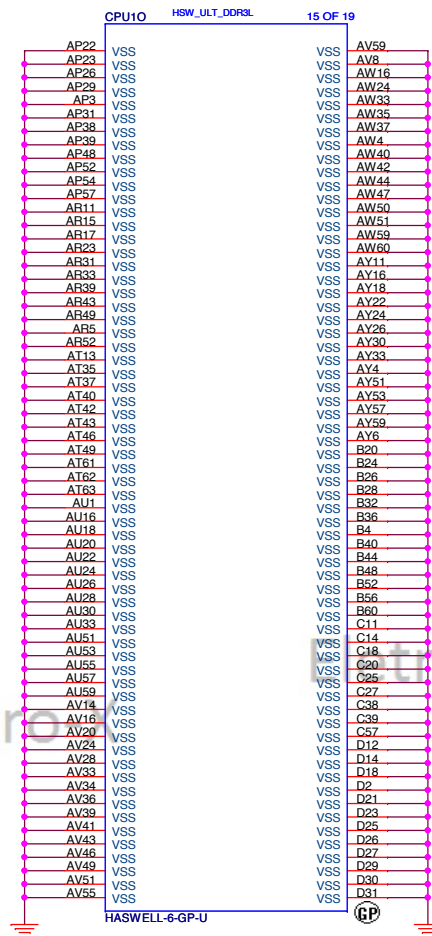
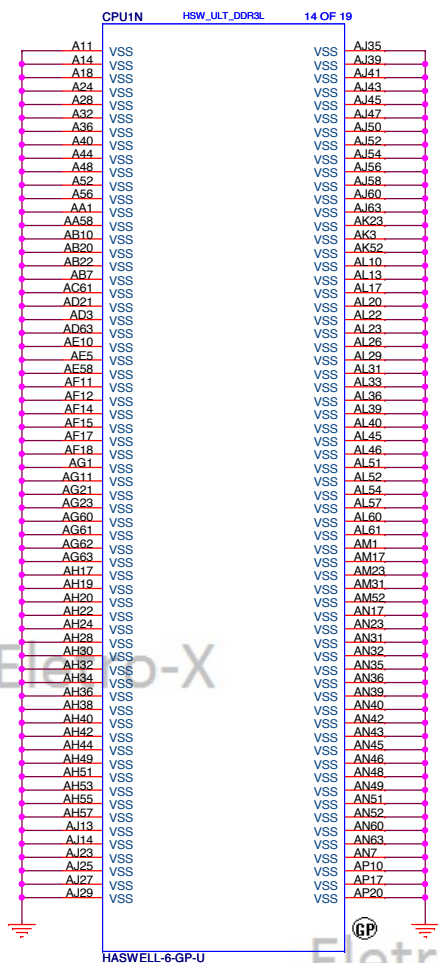




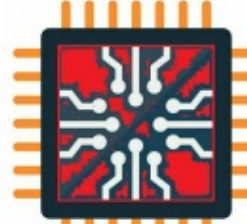
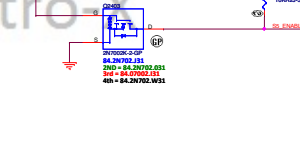
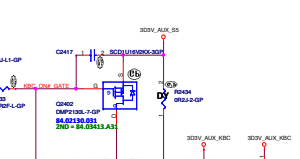
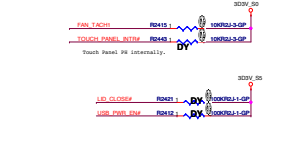
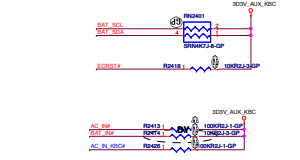
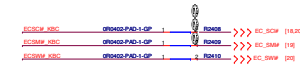
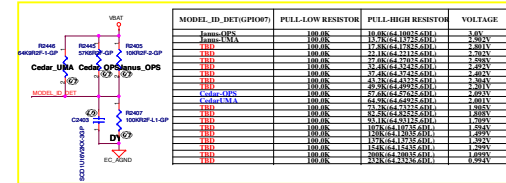
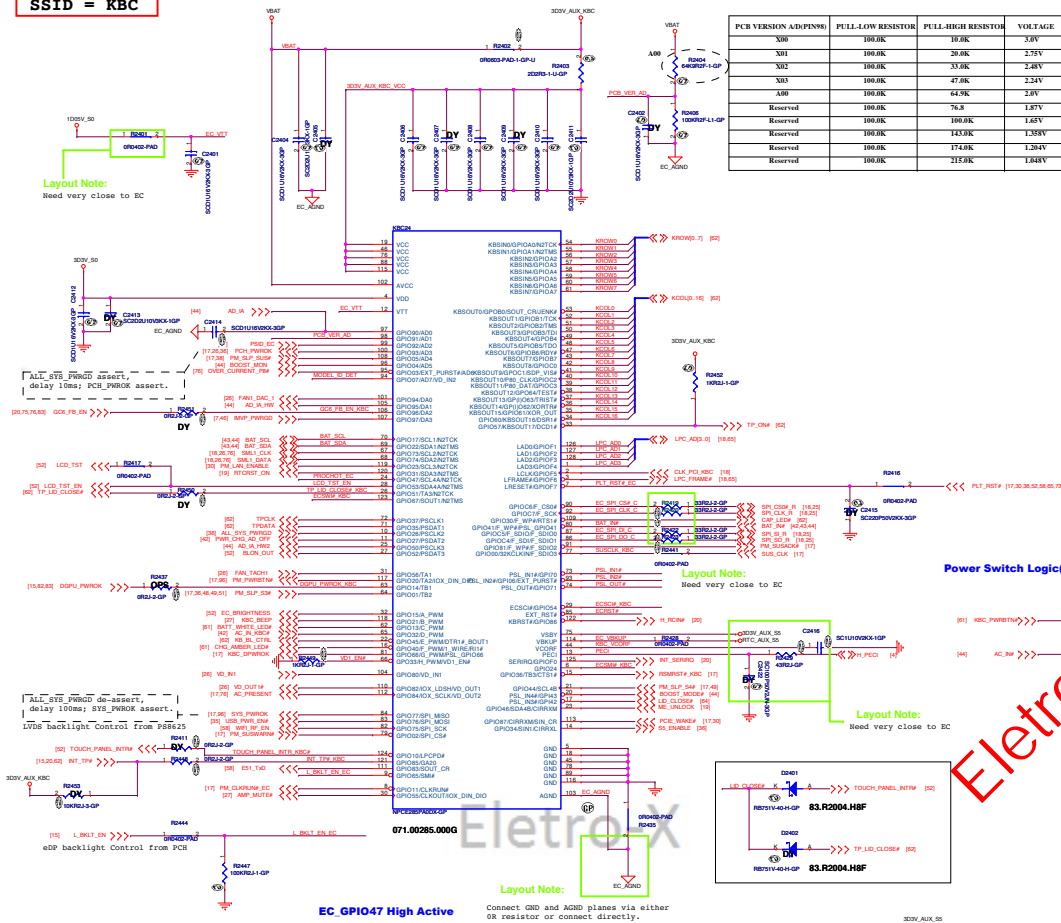
SSID = PCH



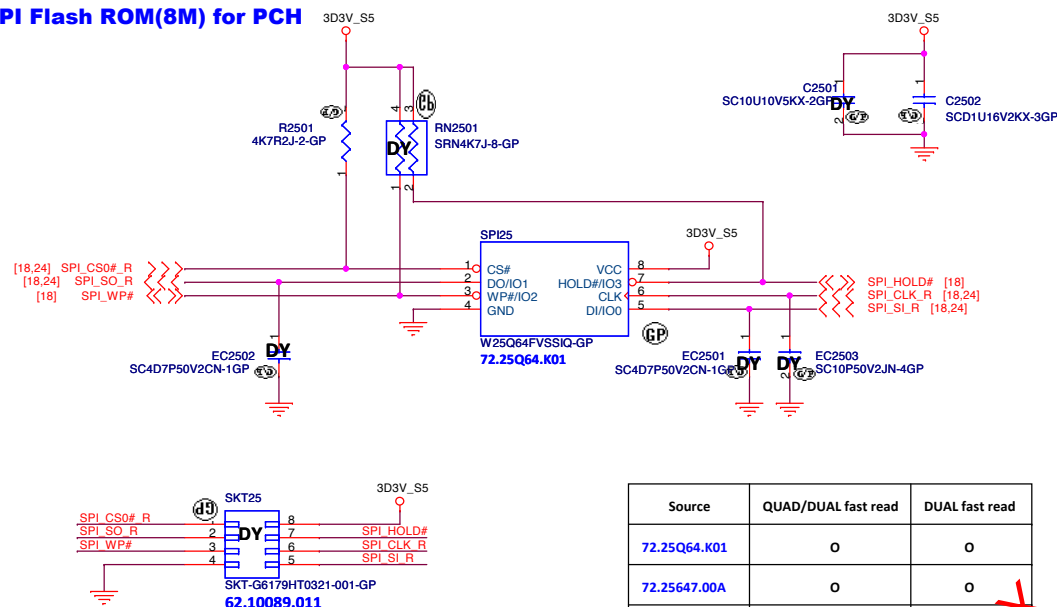
SSID = PCH



SSID = KBC

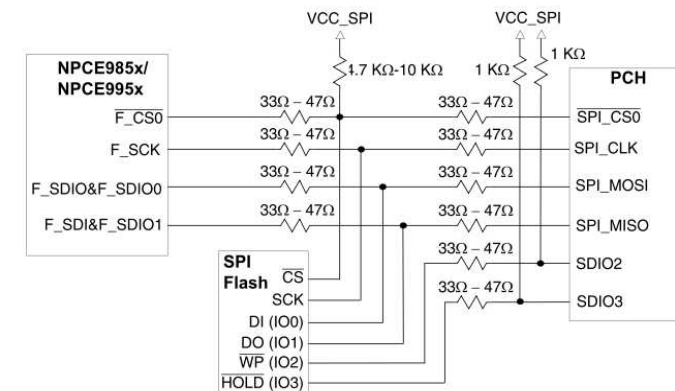


### SPI Flash ROM(8M) for PCH

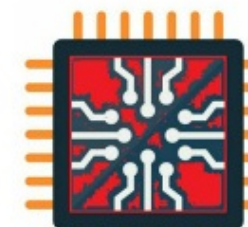
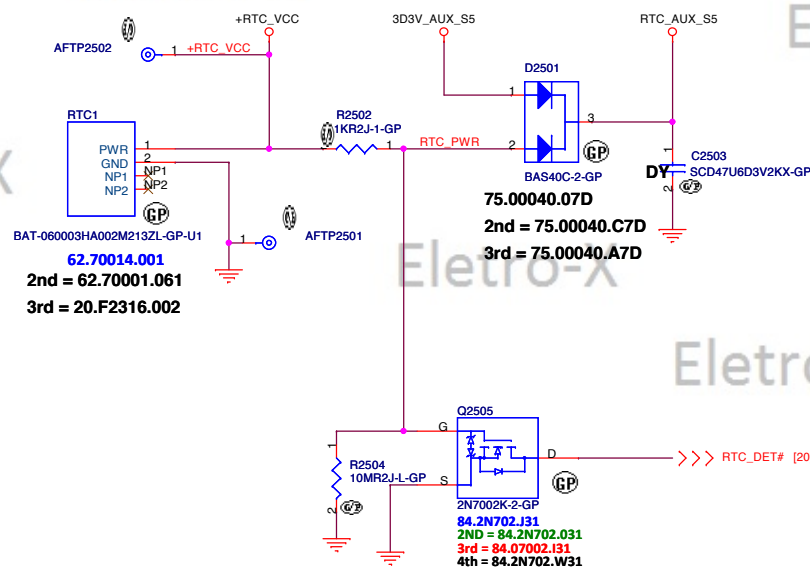


Source	QUAD/DUAL fast read	DUAL fast read
72.25Q64.K01	O	O
72.25647.00A	O	O
072.25B64.0001	O	O

### Single SPI shared flash connection (SPI Quad I/O mode)

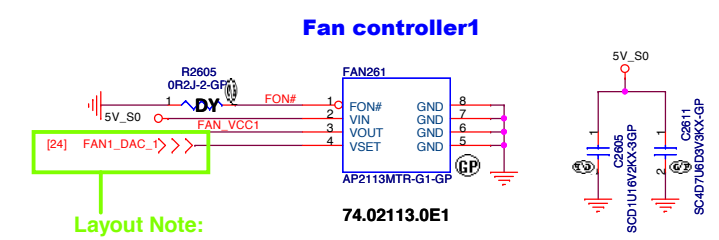
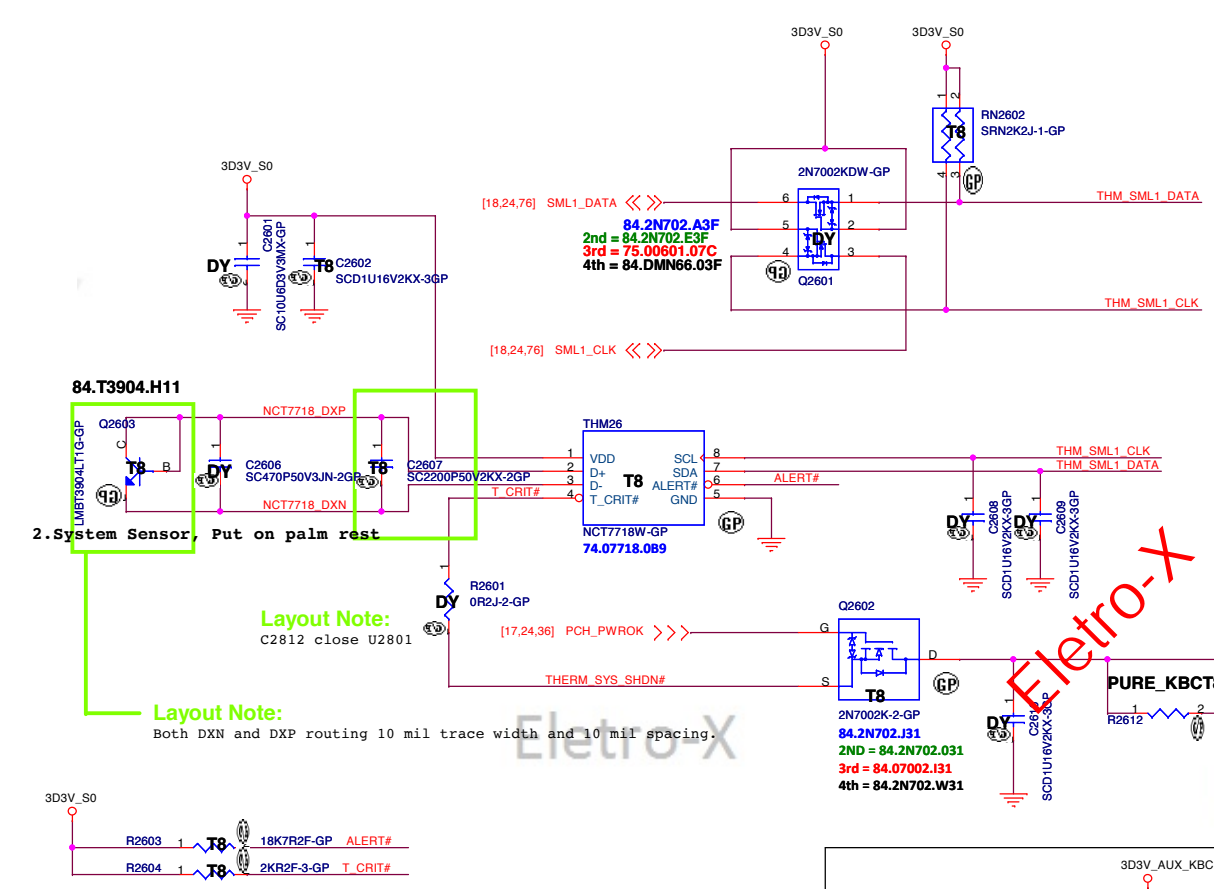


Refer to "NCPE985x/ NPCE995x board design reference guide"

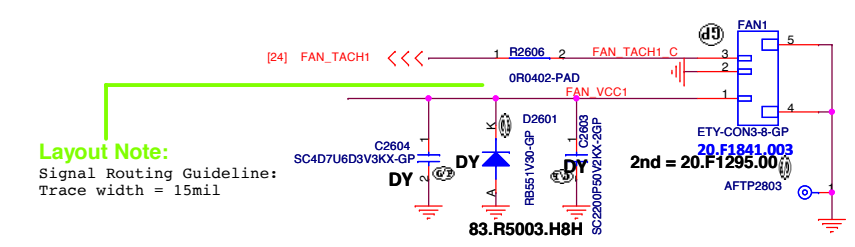
**SSID = RBATT**



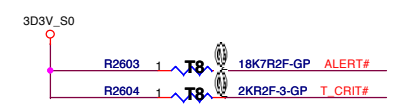
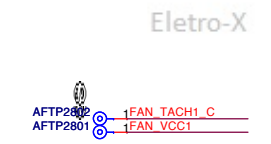
**SSID = Thermal**



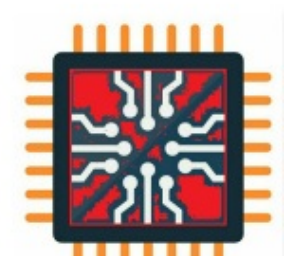
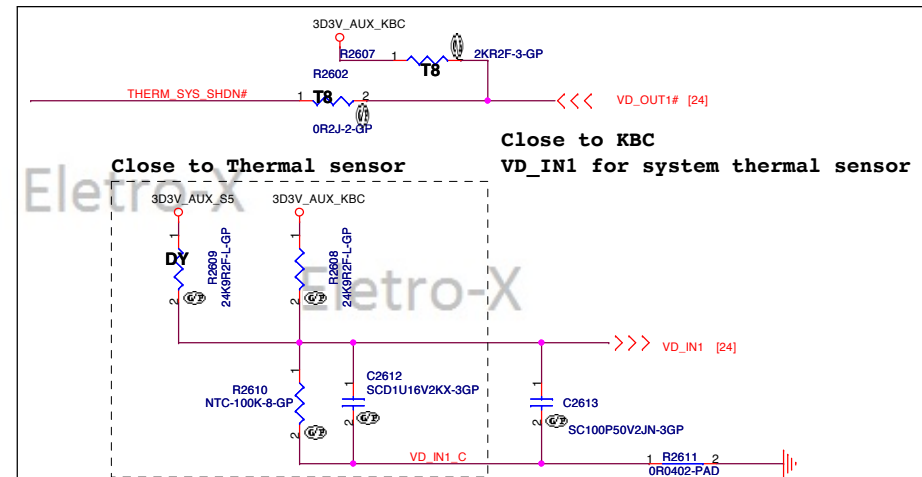
**Layout Note:**  
Need 10 mil trace width.



**Layout Note:**  
Signal Routing Guideline:  
Trace width = 15mil

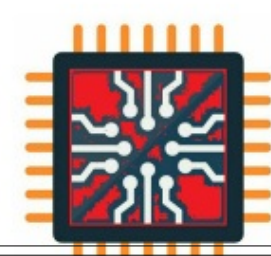


TEMPERATURE (°C)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125



Close to KBC  
VD IN1 for system thermal sensor



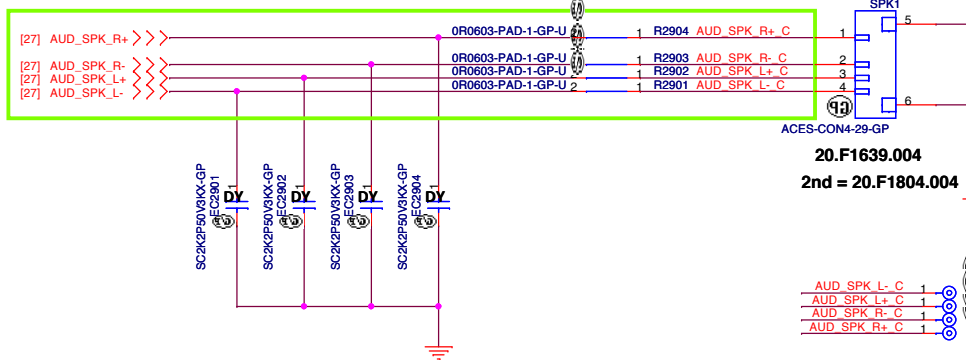


# SSID = AUDIO

## Layout Note:

Speaker trace width >40mil @ 2W4ohm speaker power

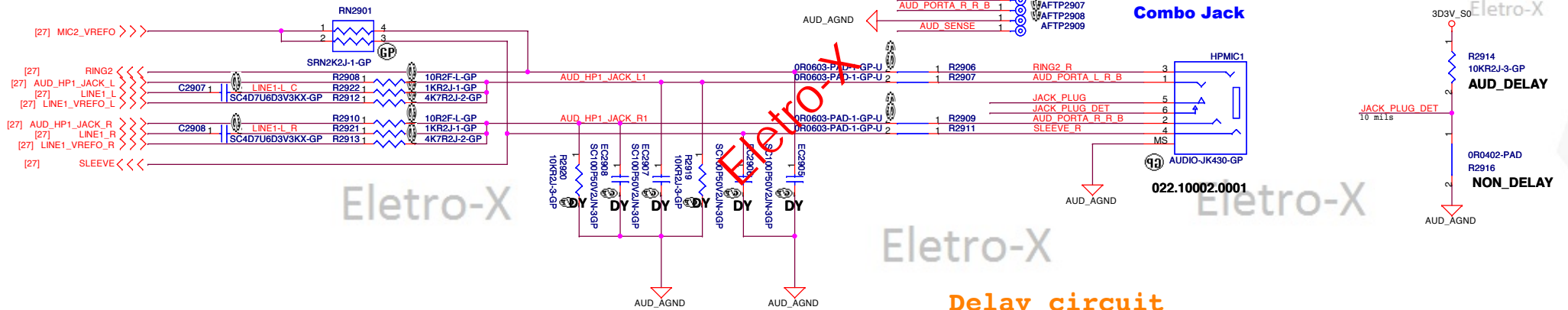
## Speaker



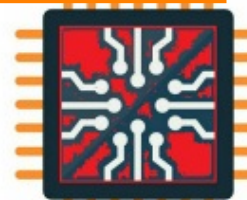
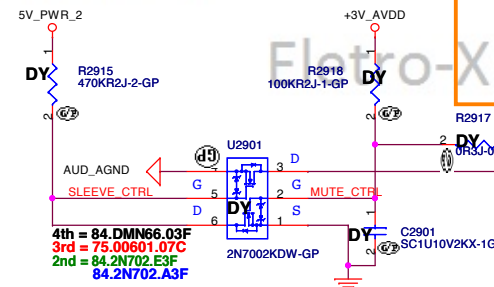
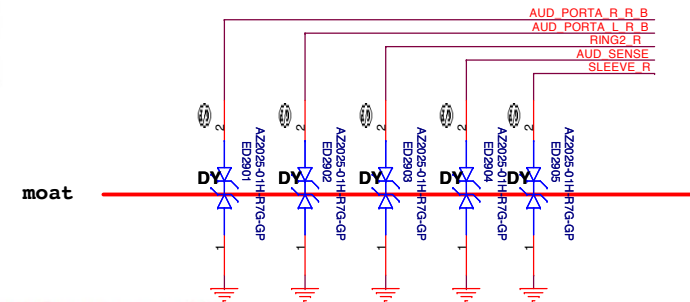
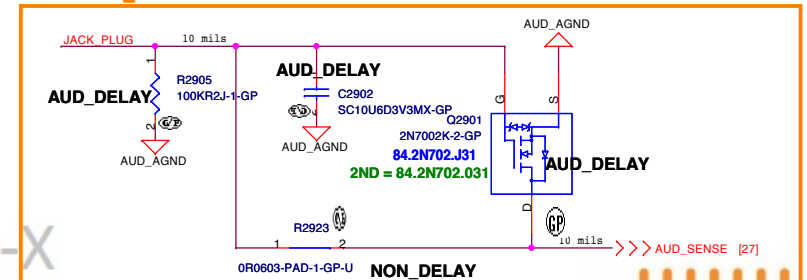
CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-

AUD\_SPK\_L- C 1  
AUD\_SPK\_L+ C 1  
AUD\_SPK\_R- C 1  
AUD\_SPK\_R+ C 1

AFTP2901  
AFTP2902  
AFTP2903  
AFTP2904



## Delay circuit

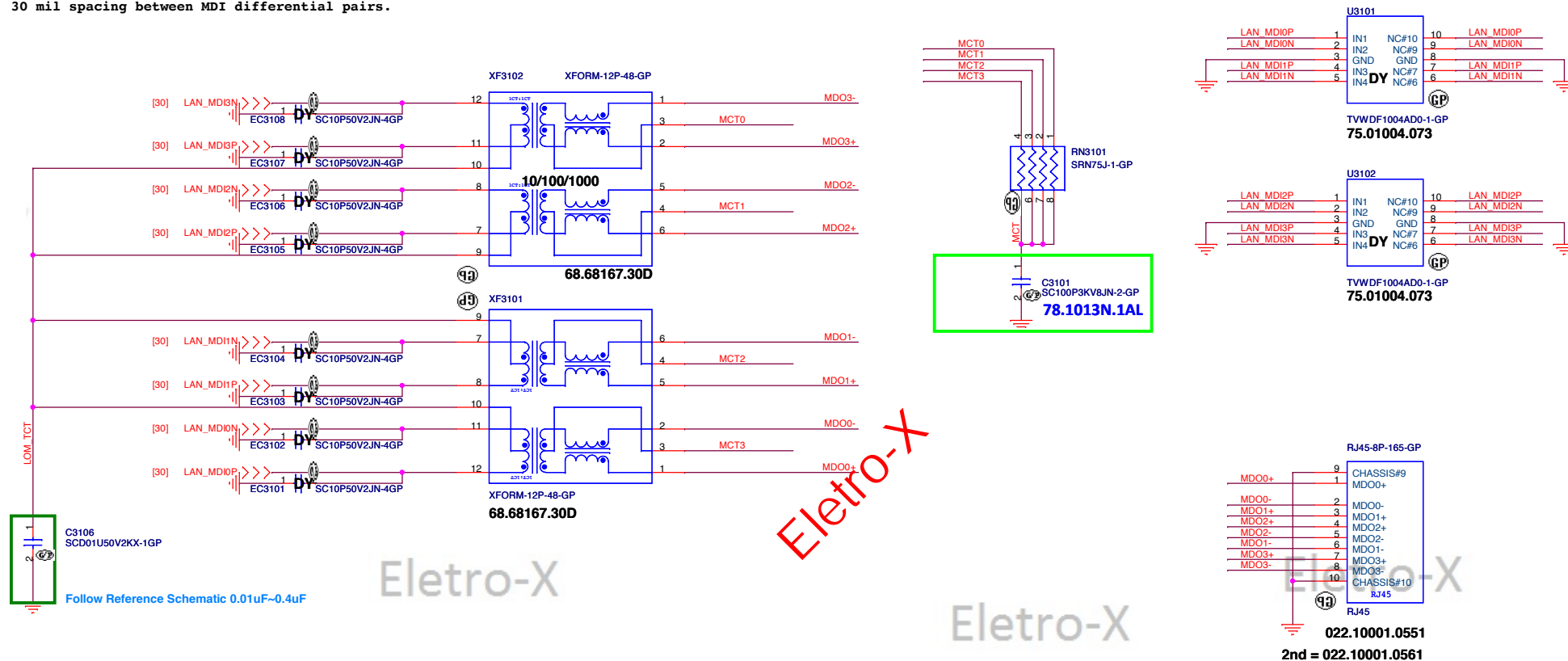




SSID = LOM

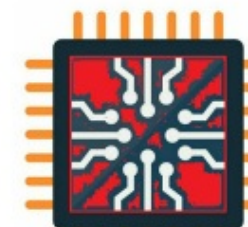
## LAN TransFormer (10/100/1000M & 10/100M co-lay)

Layout note:  
30 mil spacing between MDI differential pairs.

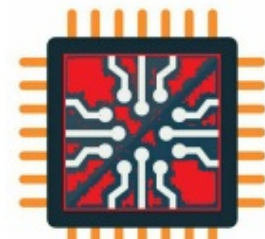
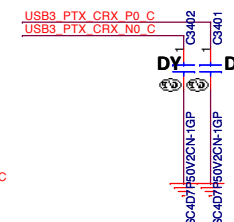
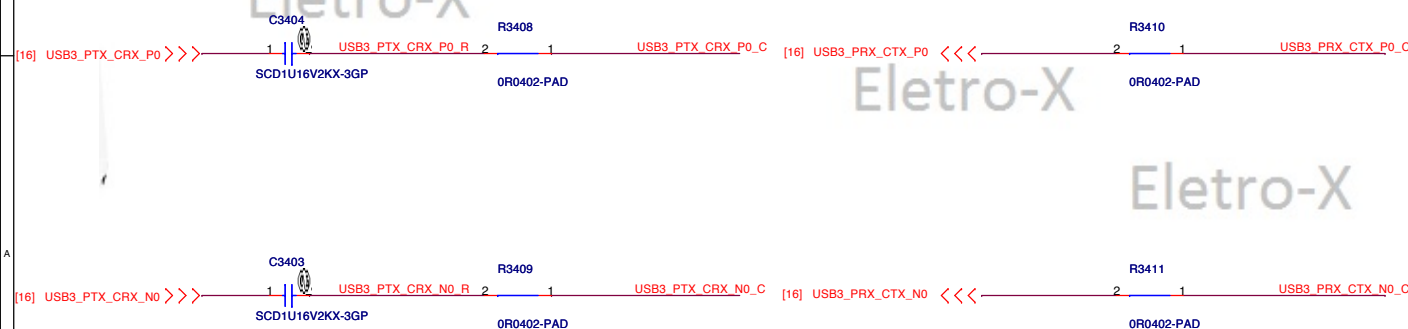
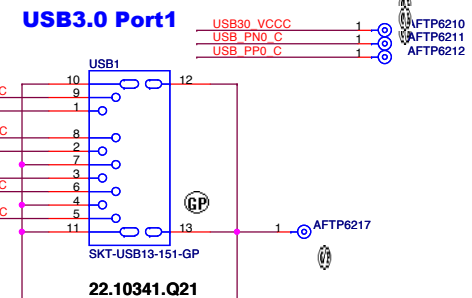
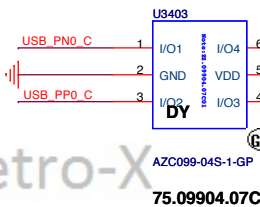
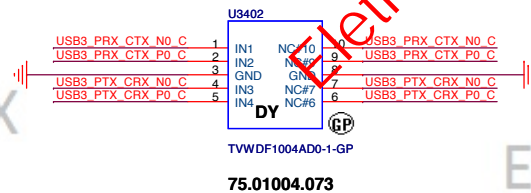
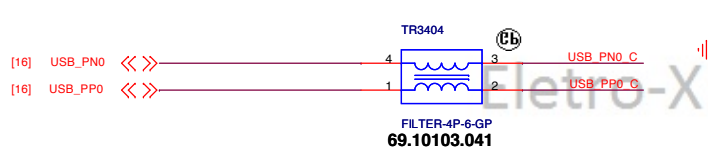
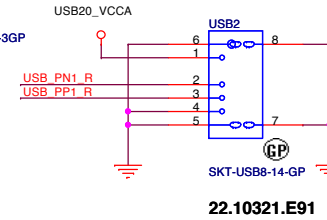
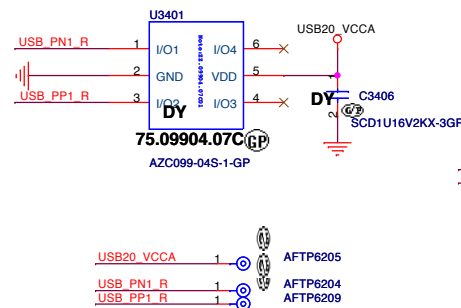


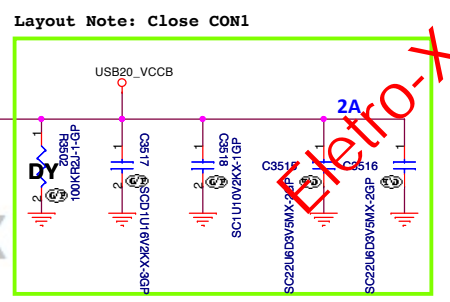
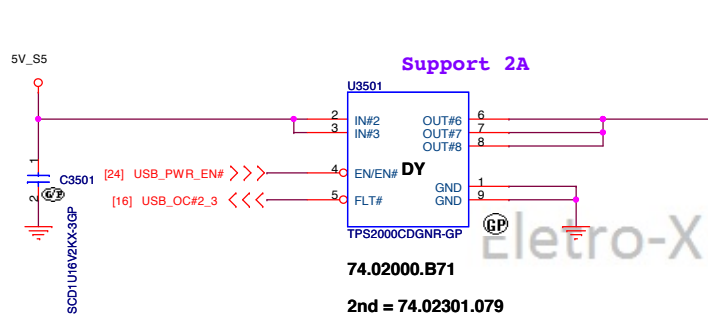
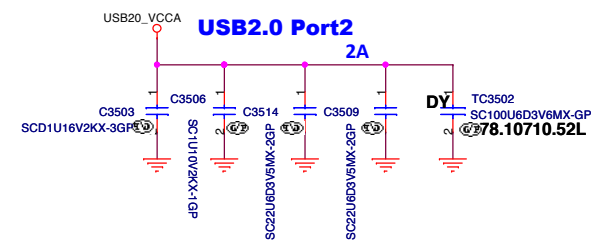
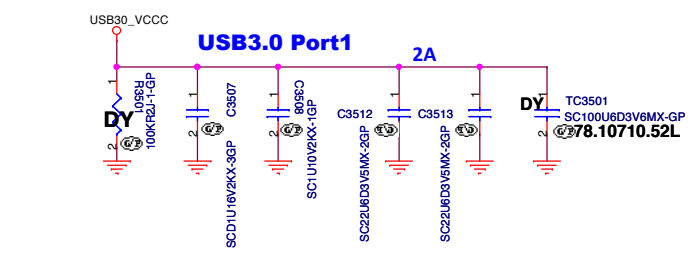
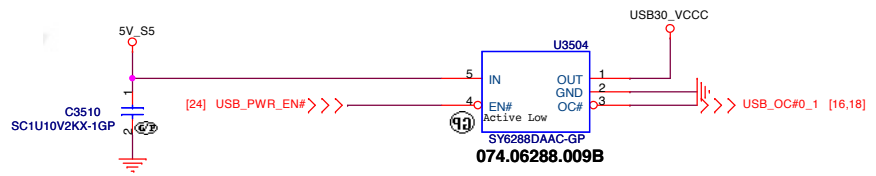
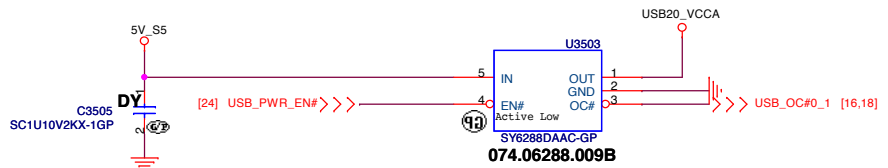
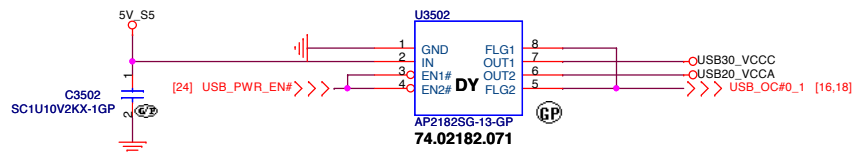
Layout:  
Place near RJ45

AFTP3107	1	MDO0+
AFTP3102	1	MDO0-
AFTP3101	1	MDO1+
AFTP3103	1	MDO1-
AFTP3104	1	MDO2+
AFTP3105	1	MDO2-
AFTP3106	1	MDO3+
AFTP3107	1	MDO3-

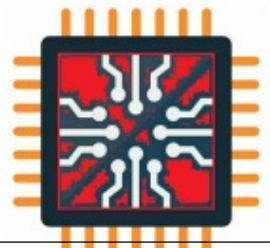
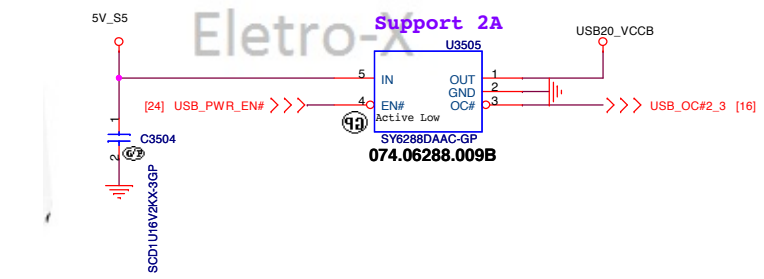


SSID = USB





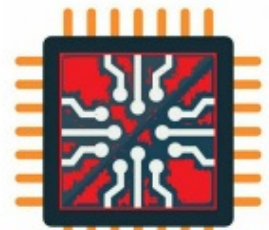
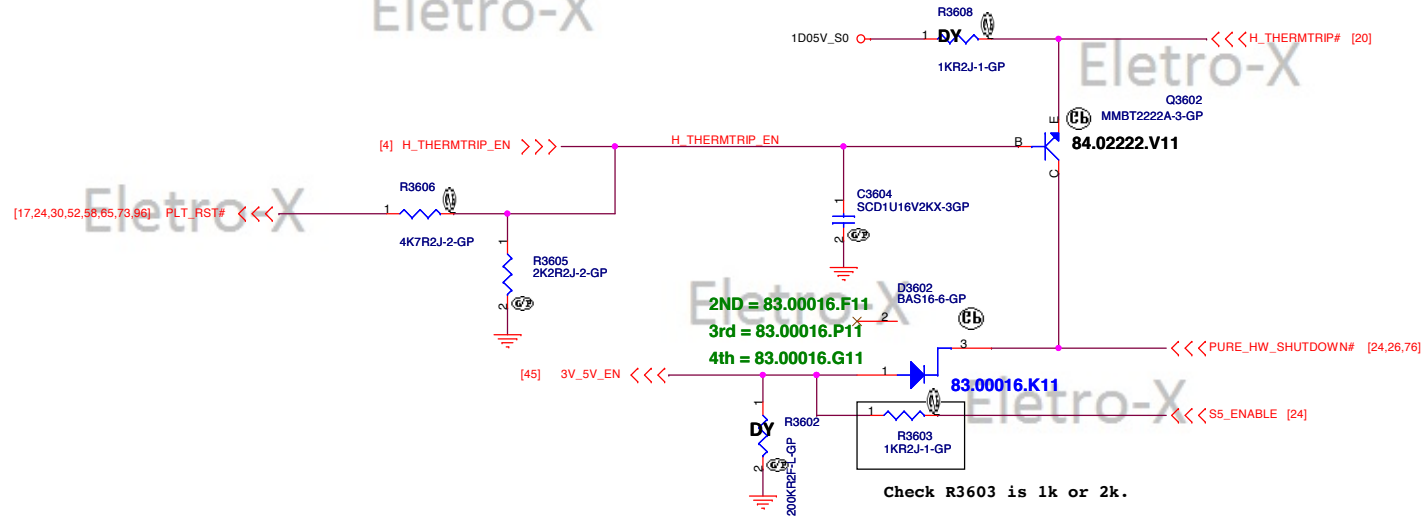
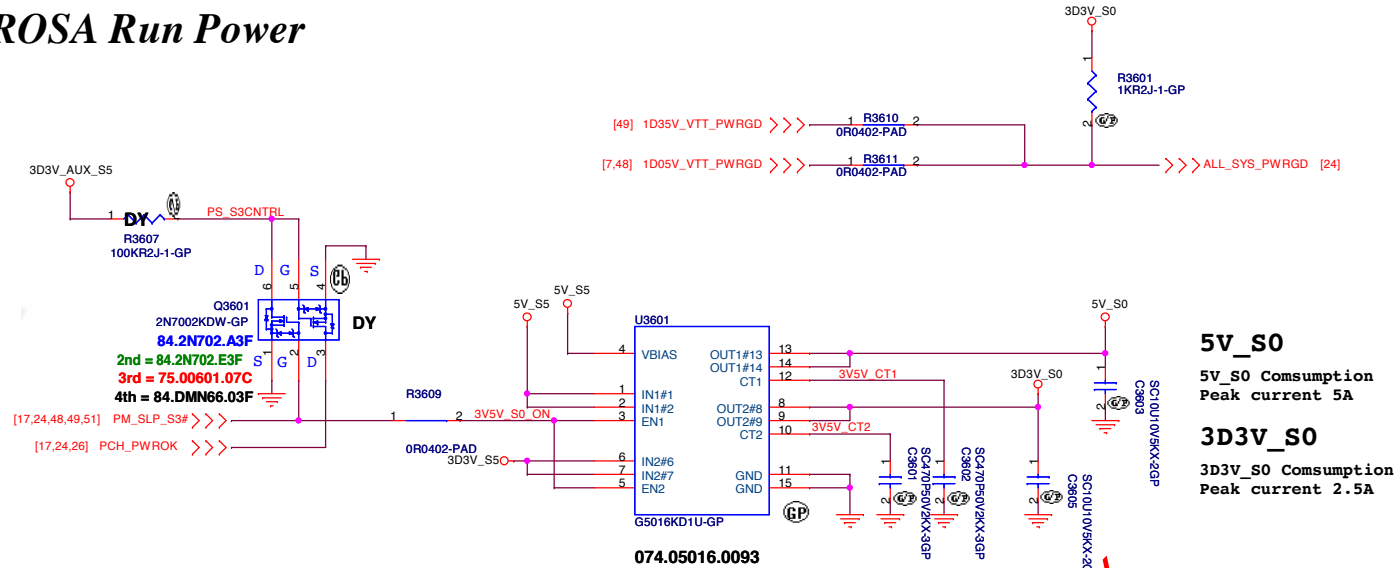
**USB2.0 Port3 (IO Board)**



**SSID = Reset.Suspend**

*Power Good*

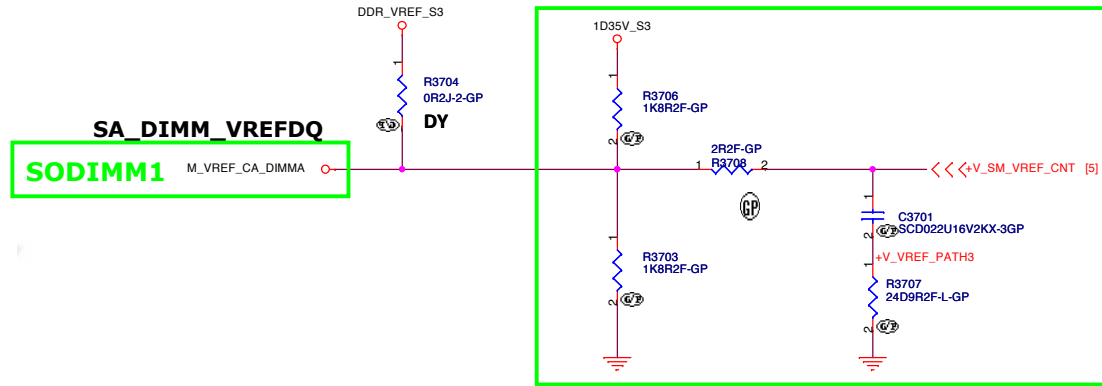
*ROSA Run Power*



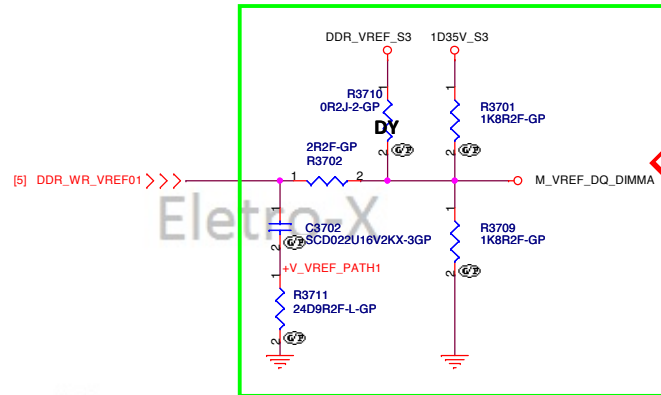


SSID = Reset.Suspend

Layout Note:  
Place Close SO-DIMM1



Layout Note:  
Place Close SO-DIMM1



Eletro-X

Eletro-X

Eletro-X

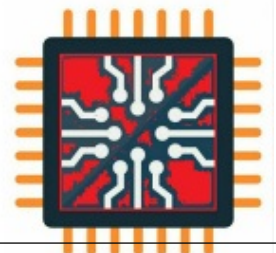
Eletro-X

Eletro-X

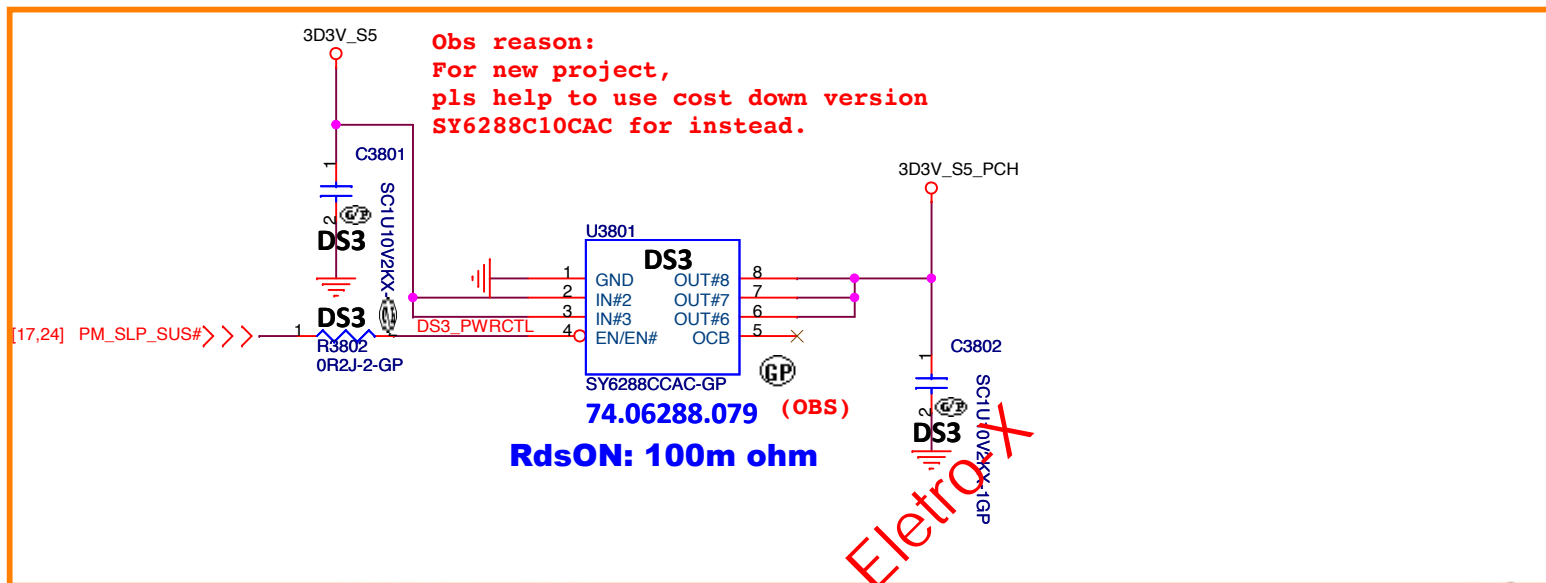
Eletro-X

Eletro-X

Eletro-X



Team Eletro-X



Eletro-X

DS3

Eletro-X

Eletro-X

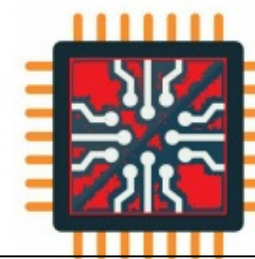
Eletro-X

Eletro-X

Eletro-X


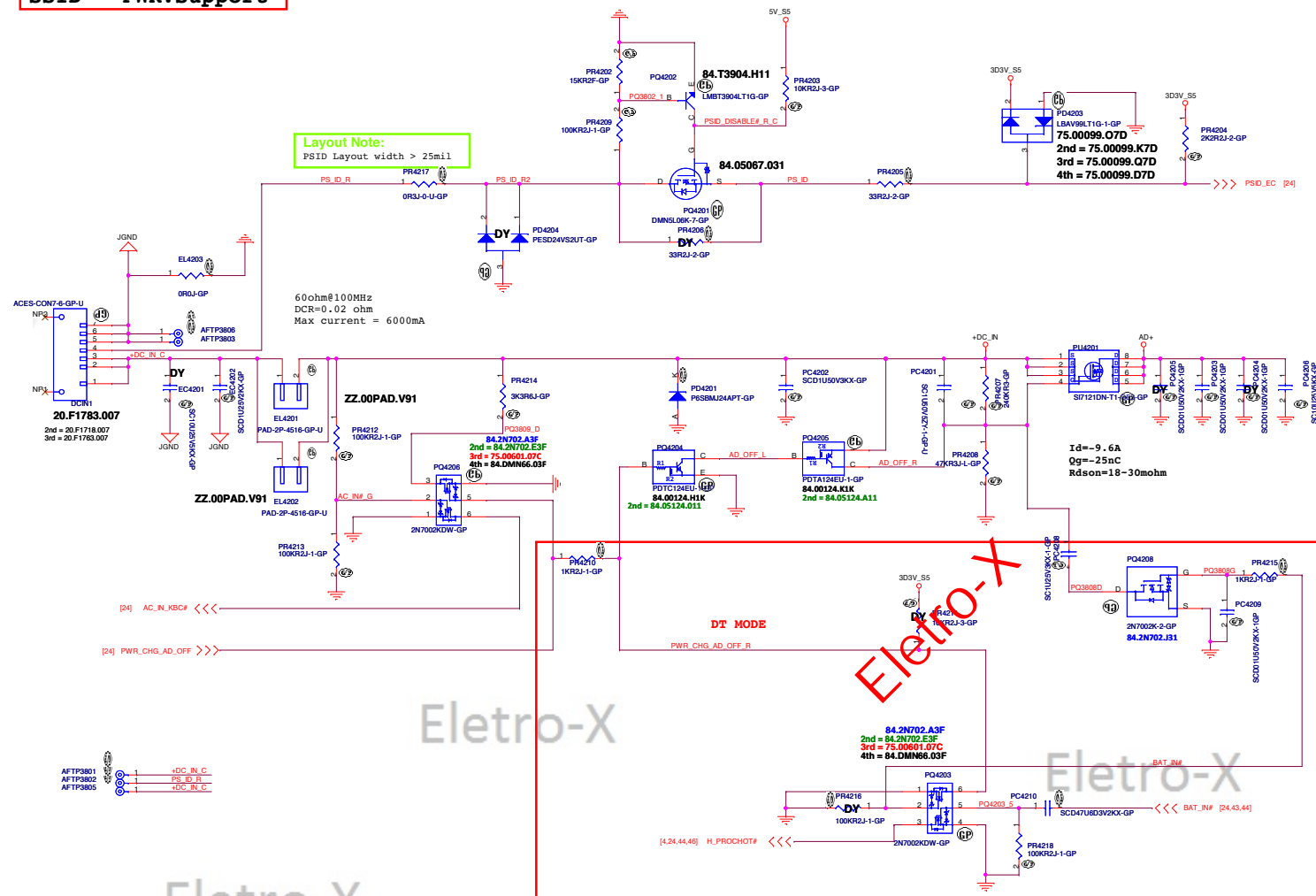
Eletro-X

Eletro-X

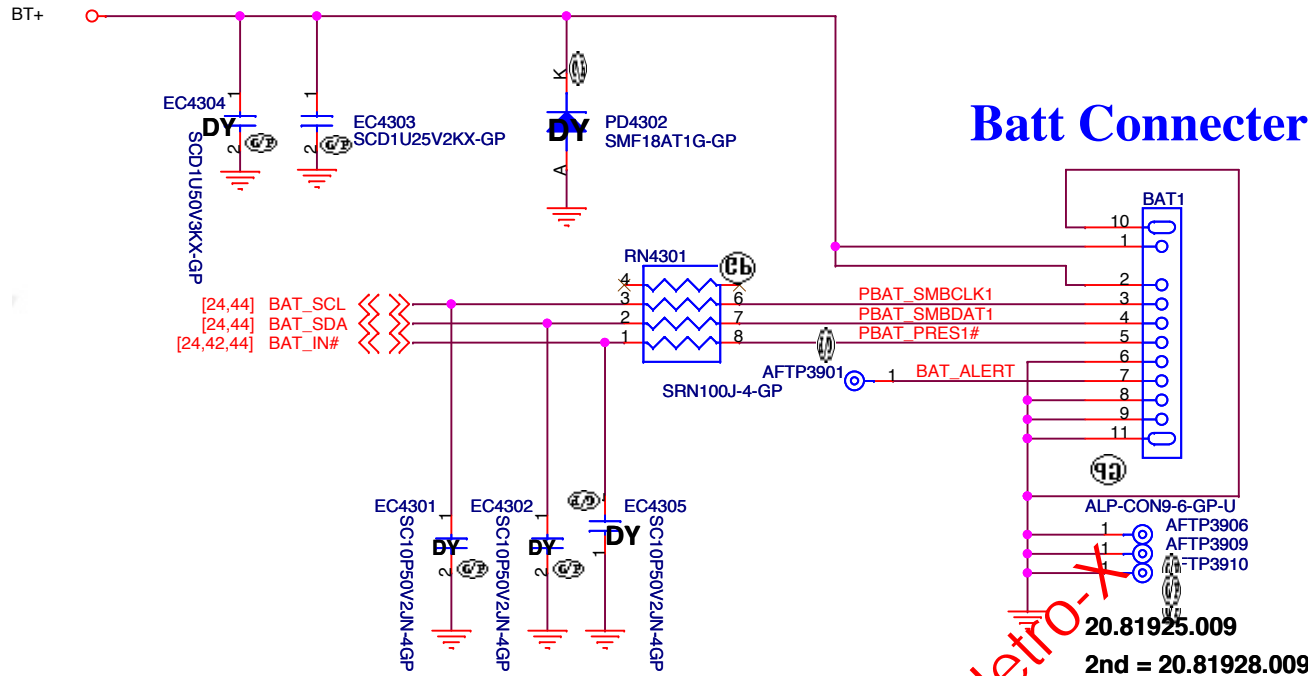


Team Eletro-X

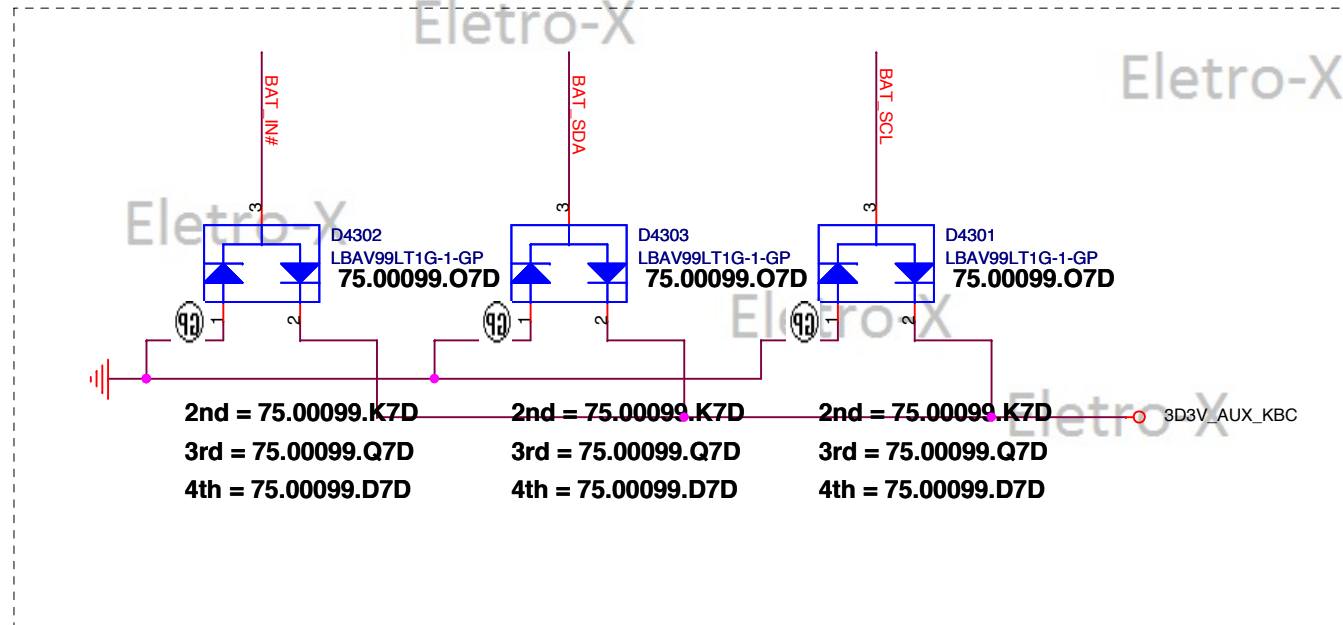
**SSID = PWR.Support**



# SSID = PWR.Support



Placement: Close to Batt Connector



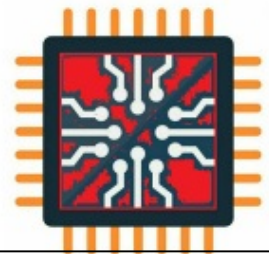
PBAT_PRES1#	1	AFTP3902
PBAT_SMBDAT1	1	AFTP3903
PBAT_SMBCLK1	1	AFTP3904
BT+	1	AFTP3905
BT+	1	AFTP3907
BT+	1	AFTP3908

Eletro-X

Eletro-X

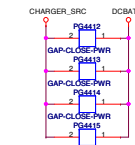
Eletro-X

Eletro-X

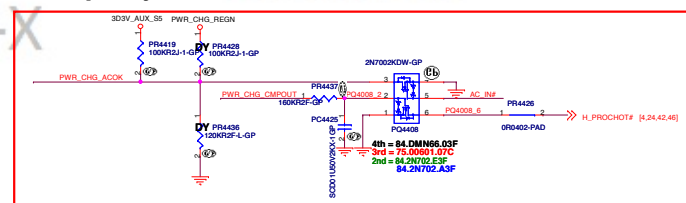


Team Eletro-X

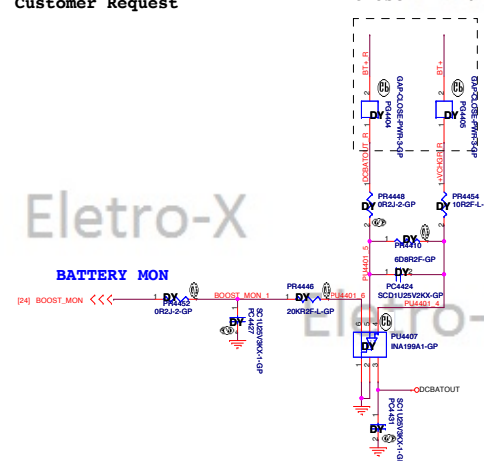
PWR\_CHG\_CMPIN  
PR4429  
150KR2F-L-GP



EE need pull high and net name

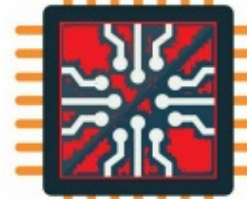


**Close PR4416**

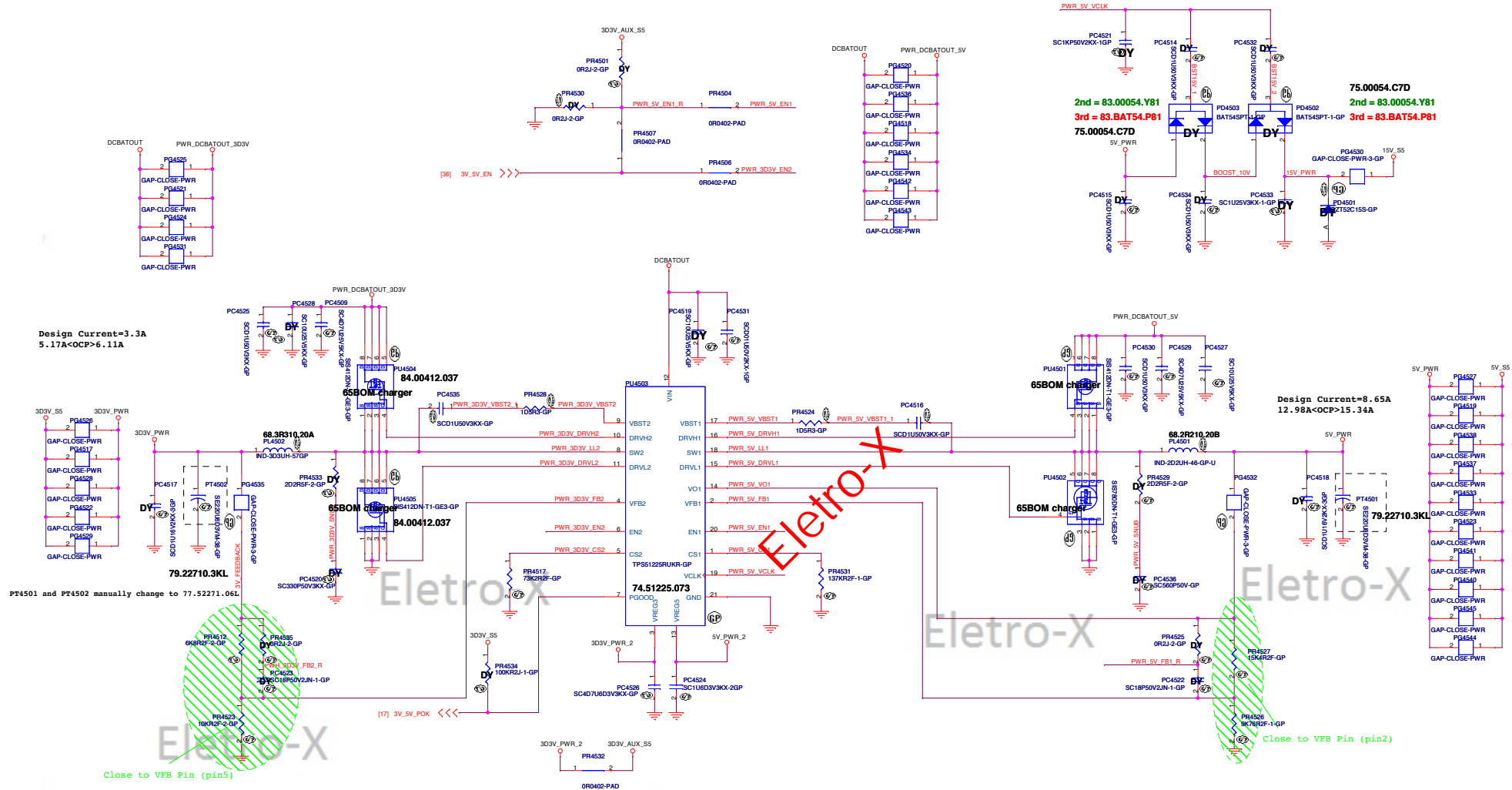


BOOST MON 1 1 DY

H_PROCHOT#	AD_IA_HW	AD_IA_HW2
45W	0	0
65W	1	0
90W	0	1



SSID = PWR.Plane.Regulator\_5v3p3v

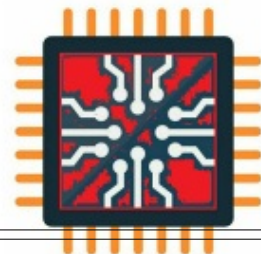


I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L  
Inductor: CHIP IND 3.3UH PCMC063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A  
O/P cap:CHIP CAP POL 220U 6.3V M 6.3\*4.5 /Matsuki/ 17mOhm / 77.52271.09L  
H/S:SIS412 / 24mOhm/30mOhm4.5Vgs / 84.00412.037  
L/S:SIS780 / 14.5mOhm/17.5mOhm4.5Vgs / 84.00780.037

TPS51225 & TPS51285 Co-Lay

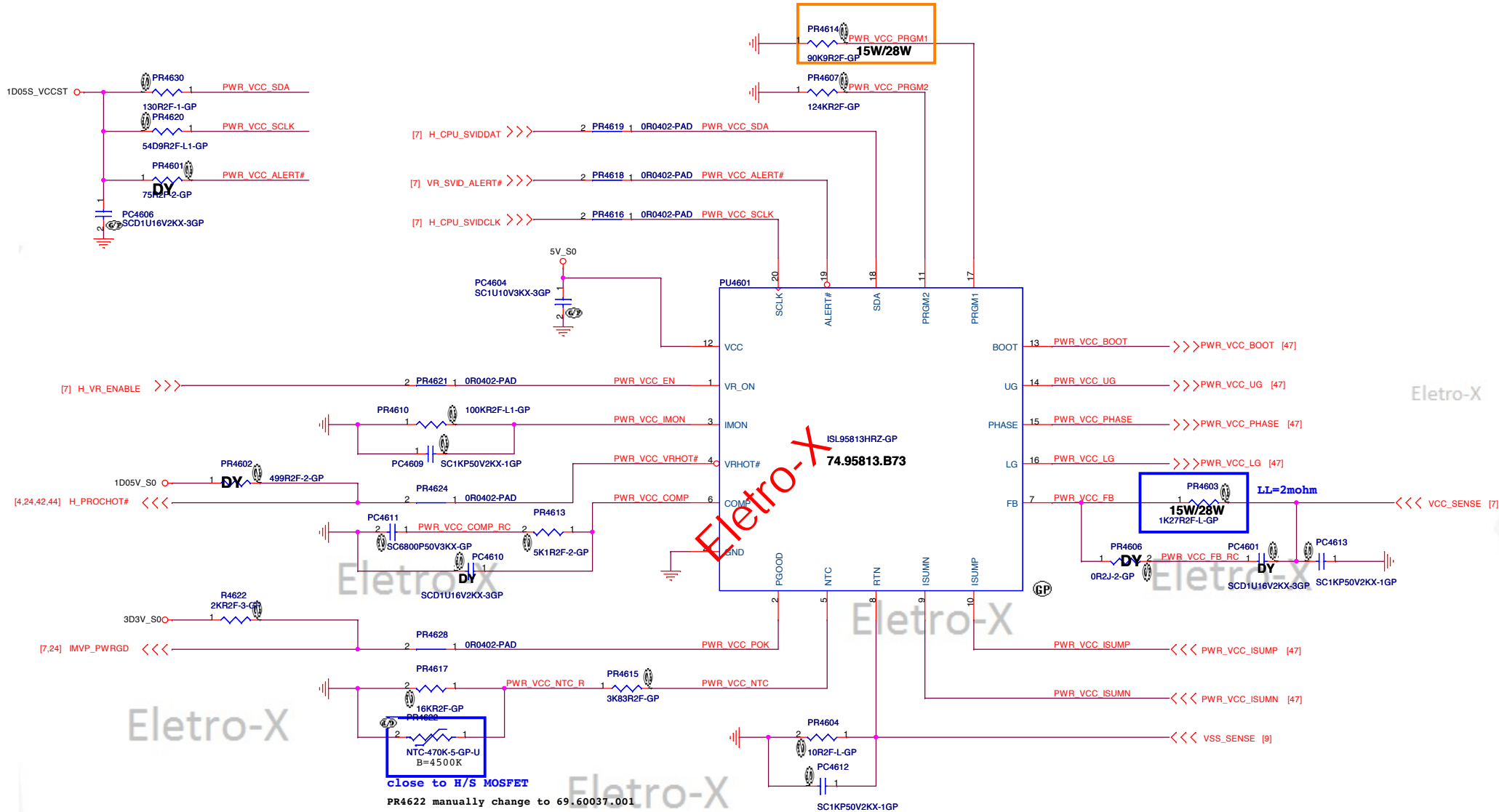
	TPS51225	TPS51285
PR4510	45.3KK	9.09K
PR4511	110K	22.1K

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L  
Inductor: CHIP CHOKe 2.2U PCMC063T-2R2MN 18mohm/20mohm Isat =14Arms 68.2R210.20B  
O/P cap:CHIP CAP POL 220U 6.3V M 6.3\*4.5 /Matsuki/ 17mOhm / 77.52271.09L  
H/S:SIS412 / 24mOhm/30mOhm4.5Vgs / 84.00412.037  
L/S:SIS780 / 14.5mOhm/17.5mOhm4.5Vgs / 84.00780.037



Team Eletro-X

# SSID = CPU.Regulator

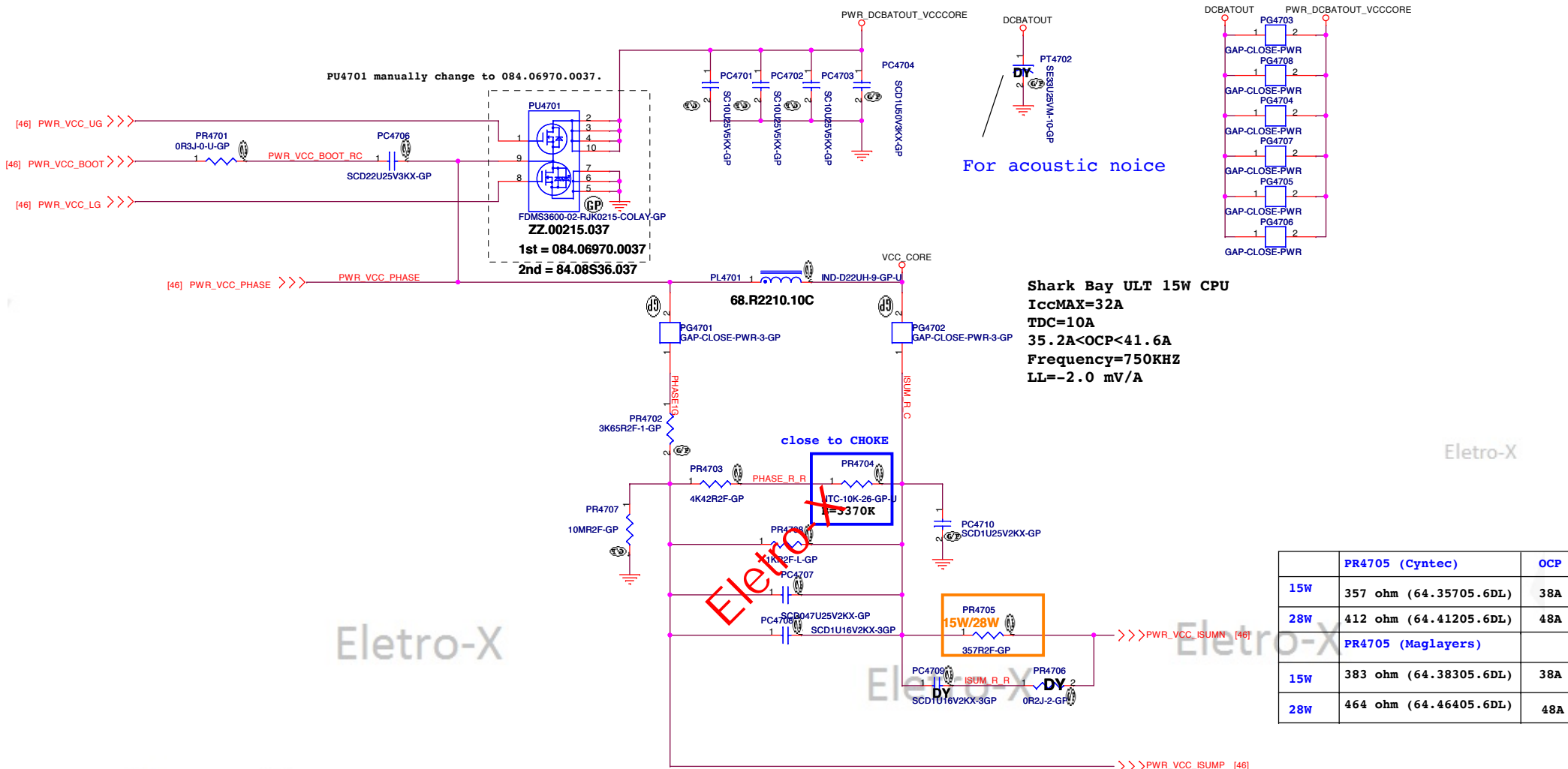


close to H/S MOSFET  
PR4622 manually change to 69.60037.001

	PR4603	PR4614
15W	1.27K 64.12715.6DL	90.9K 64.90925.6DL
28W	1.58K 64.15815.6DL	113K 64.11335.6DL

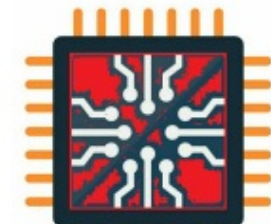
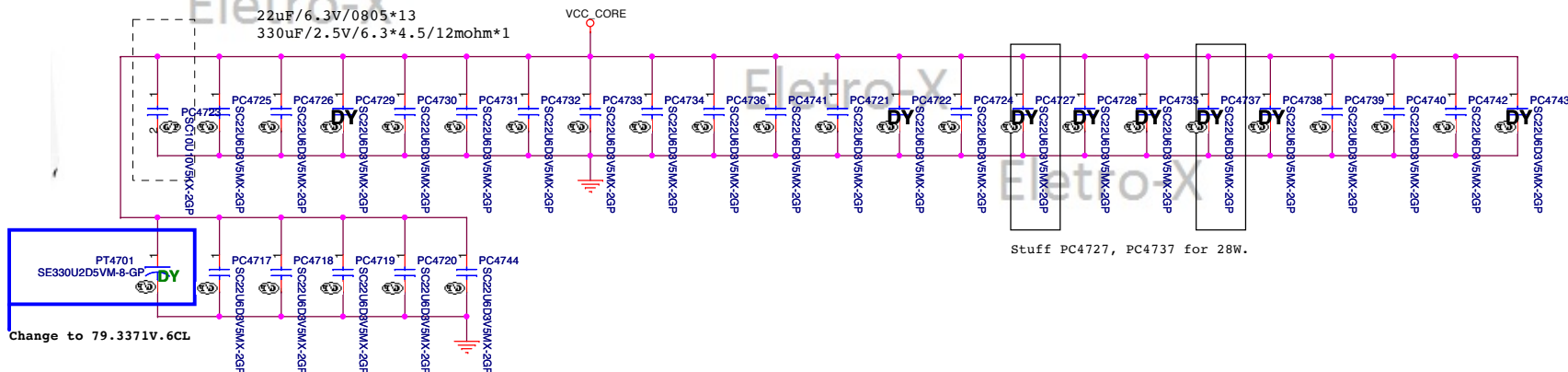




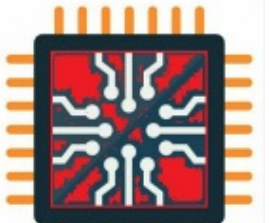
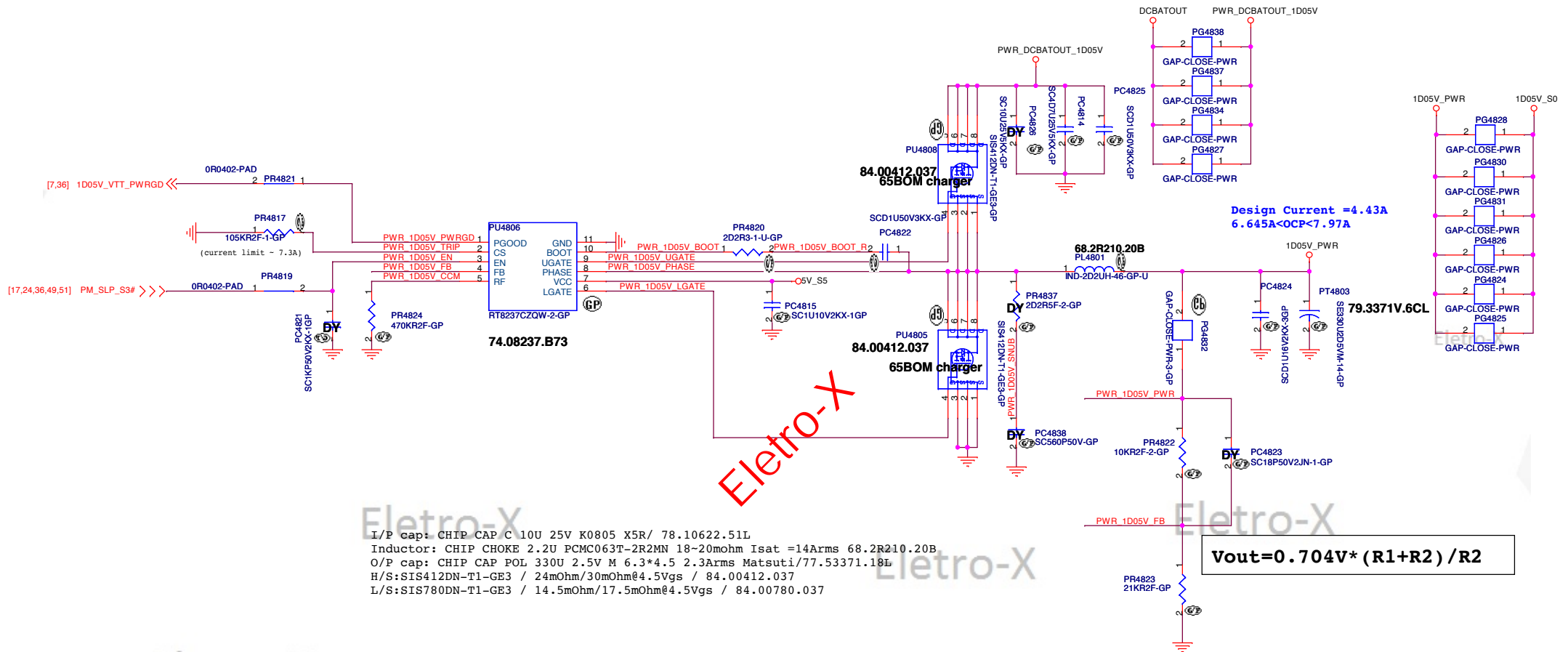


Change PC4723 to 100U from 22U based on PI Simulation.

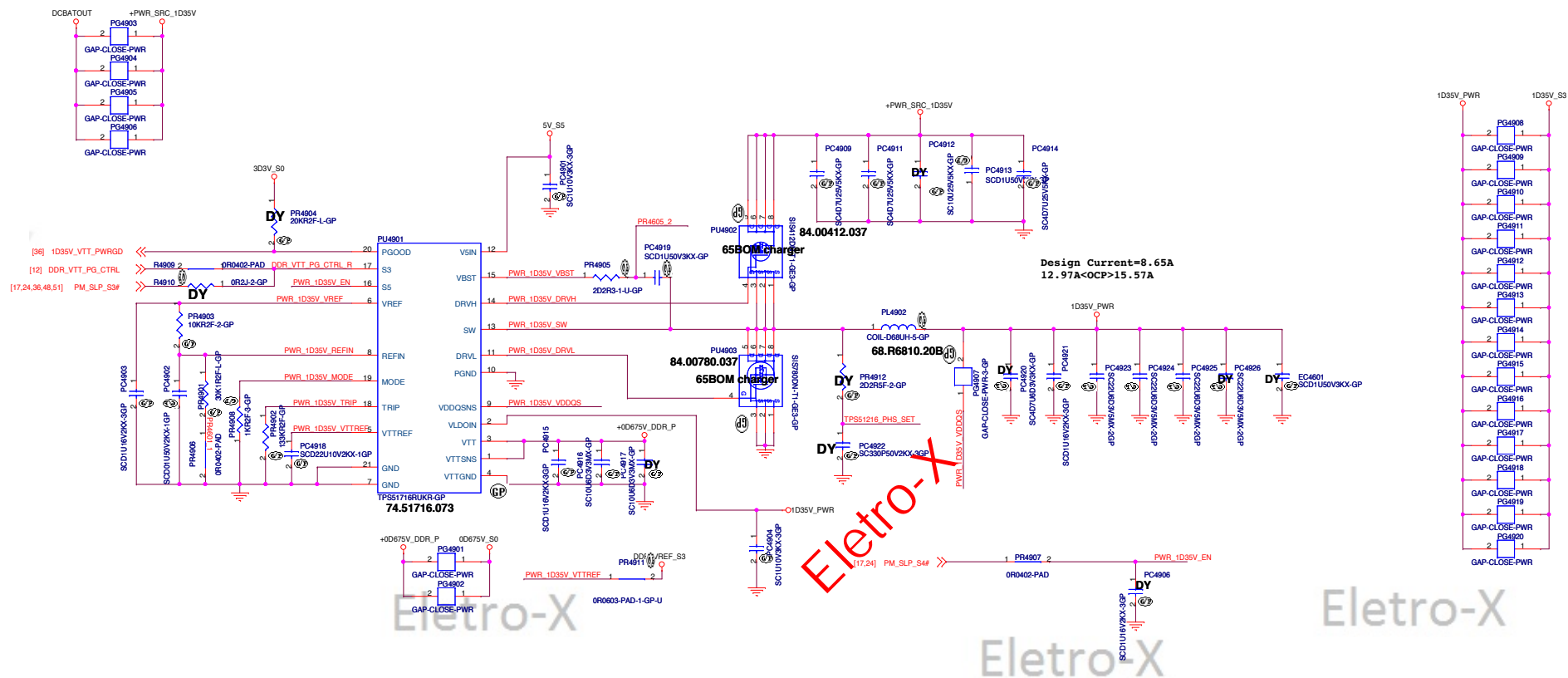
22uF/6.3V/0805\*13  
 330uF/2.5V/6.3\*4.5/12mohm\*1



SSID = PWR.Plane.Regulator\_1p05v

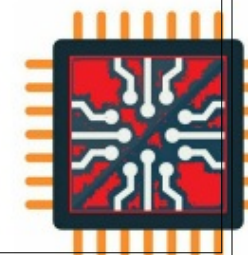


```
SSID = PWR.Plane.Regulator 1p35v0p675v
```



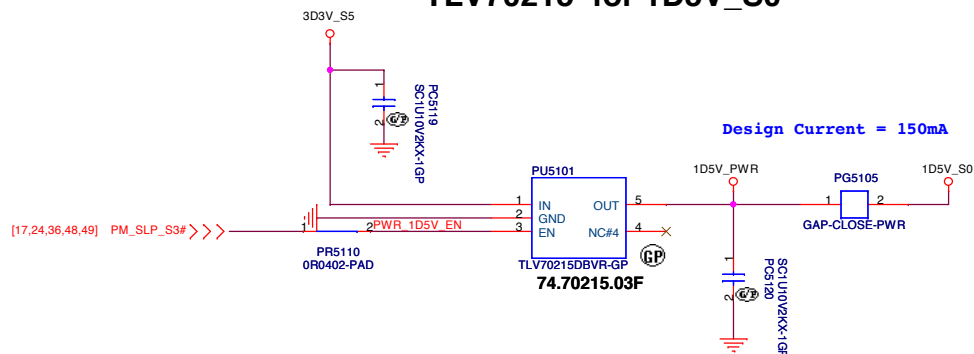
State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L  
Inductor: CHIP IND 0.1UH M PCMC063T-R10MN 1.5-1.7mohm Isat =60Arms 68.R1010.10T  
O/P cap: CHIP CAP POL 330U 2.5V M 6.3\*4.5 2.3Arms Matsui/77.53371.18L  
MOS: FET MOS FDMS3664S NC POWER56 / 84.03664.037 / Q1: 8.5-11mohm @Vgs=4.5V Q2: 2.6-3.2mohm @Vgs=4.5V

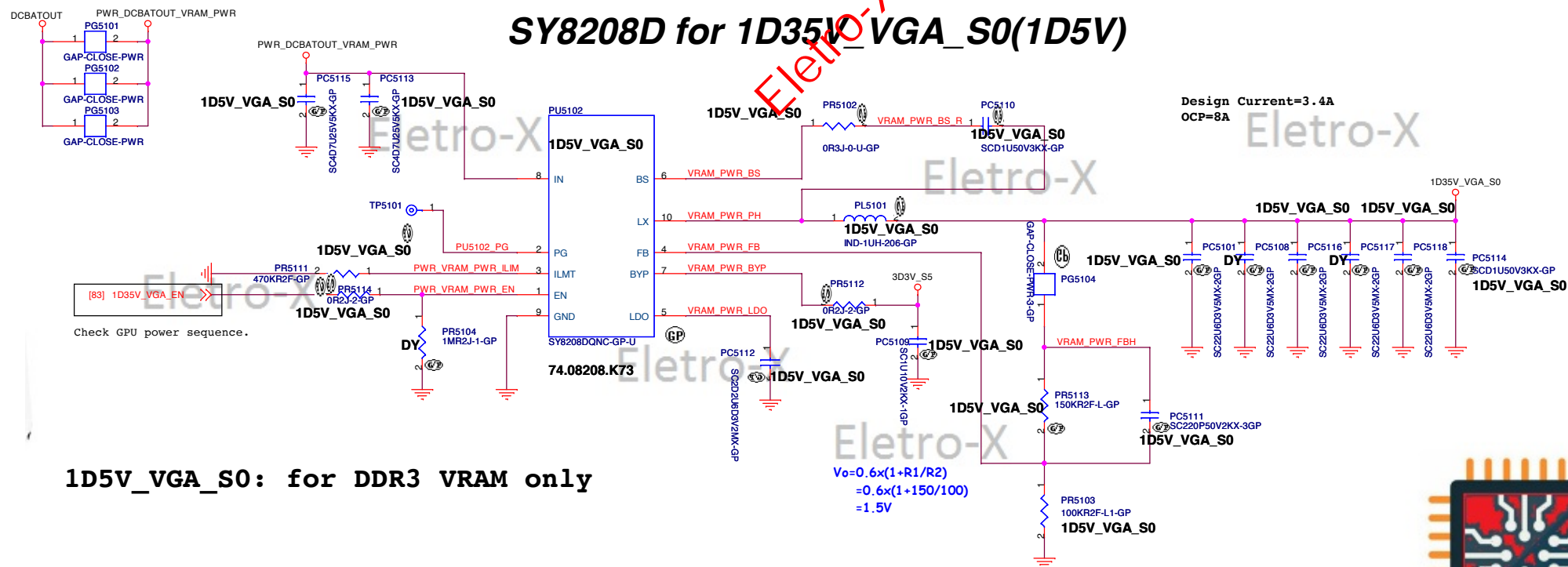


```
SSID = PWR.Plane.Regulator_1p5v
```

## TLV70215 for 1D5V\_S0



***SY8208D for 1D35V\_VGA\_S0(1D5V)***



**1D5V\_VGA\_S0: for DDR3 VRAM only**

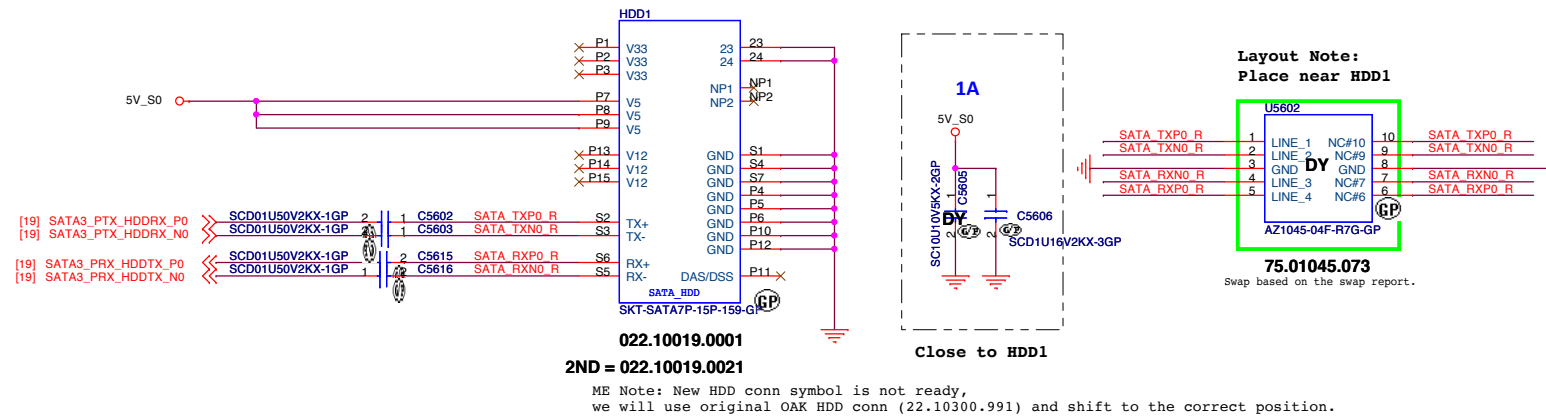
$$\begin{aligned} V_o &= 0.6 \times (1 + R_1/R_2) \\ &= 0.6 \times (1 + 150/100) \\ &= 1.5V \end{aligned}$$



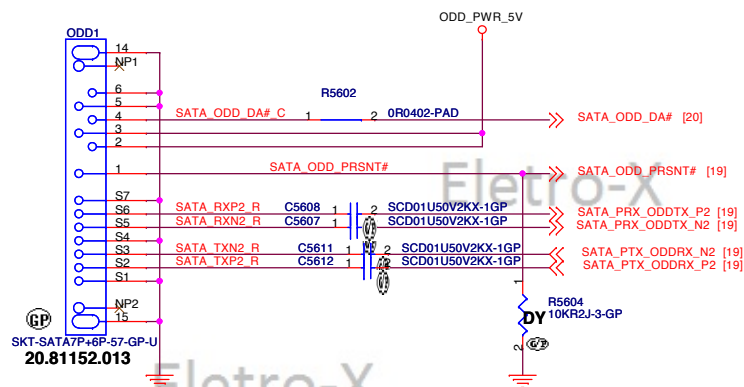


**SSID = SATA**

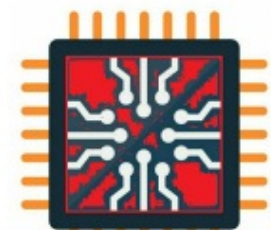
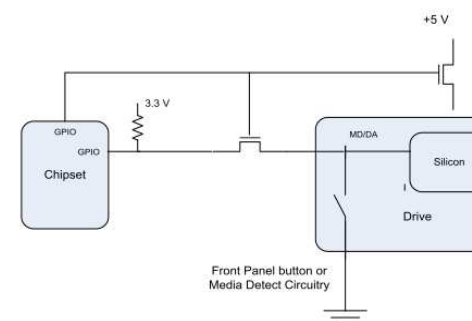
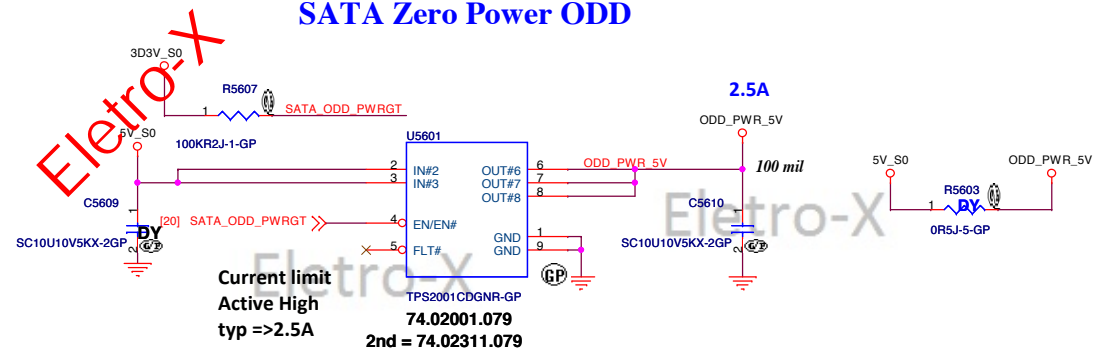
## SATA HDD Connector



## ODD Connector



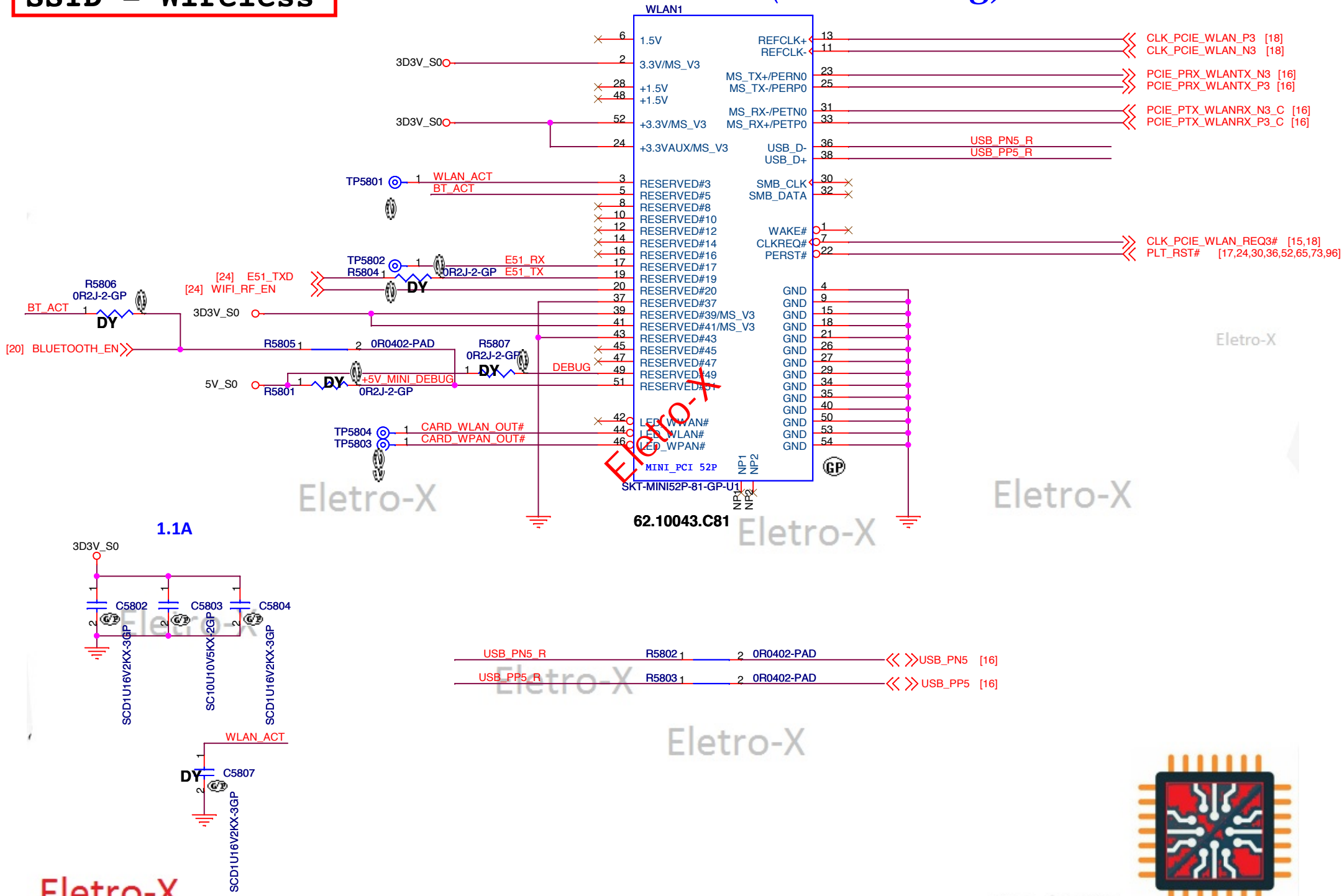
## SATA Zero Power ODD





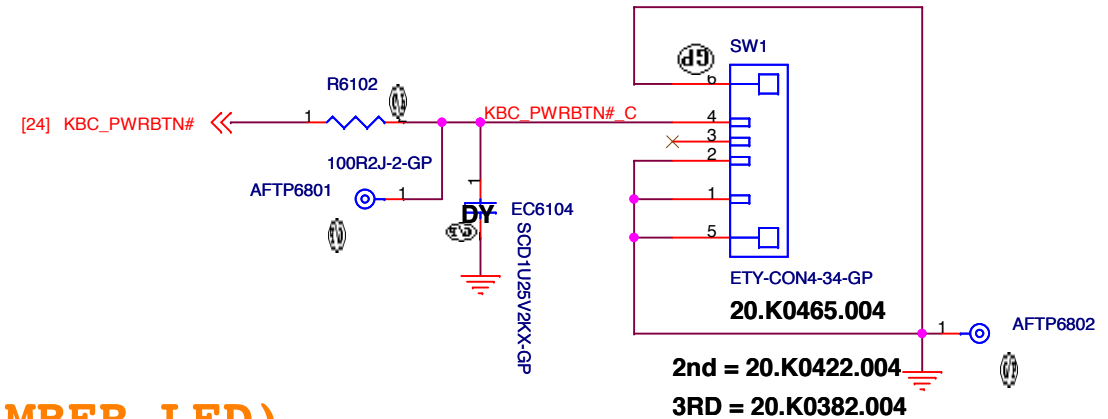
SSID = Wireless

# Mini Card Connector(802.11a/b/g)

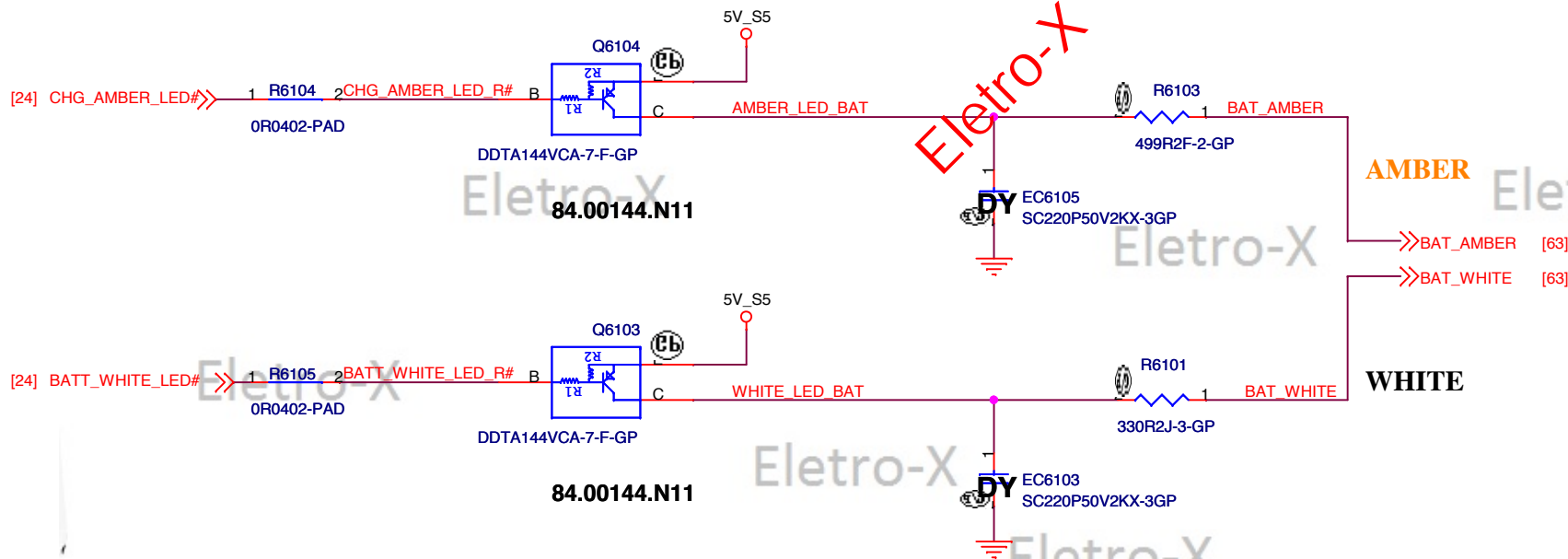


SSID = User.Interface

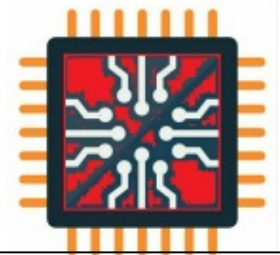
## Power button



## Battery LED1 (AMBER\_LED) Low activated from KBC GPIO

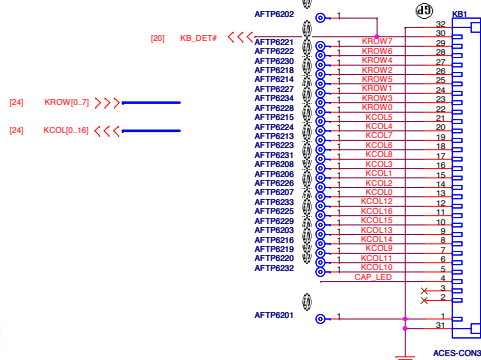


## Battery LED2 (WHITE\_LED) Low activated from KBC GPIO



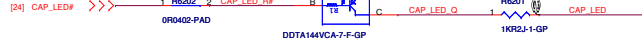
SSID = KBC

### Internal Keyboard Connector (DVC40)



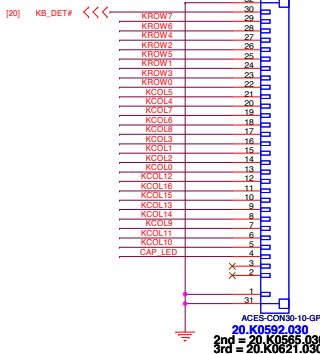
20.K0592.030  
2nd = 20.K0565.030  
3rd = 20.K0621.030

### CAP LED Control LOW acted from KBC GPIO



84.00144.N11

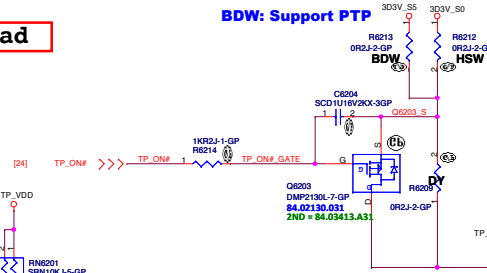
### Internal Keyboard Connector (DVC50/DVC70)



20.K0592.030  
2nd = 20.K0565.030  
3rd = 20.K0621.030

SSID = Touch.Pad

### BDW: Support PTP

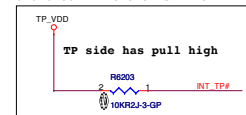


### Touch Pad Connector

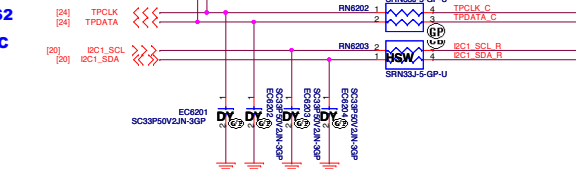
Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(P52)
8	CLK(P52)

20.K0665.008  
2nd = 20.K0667.008

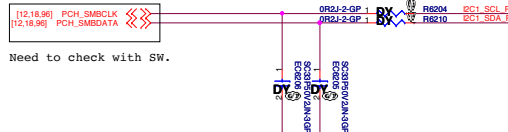
Need to check if it is Active High or Active Low  
and check if there is PH on TPAD side.



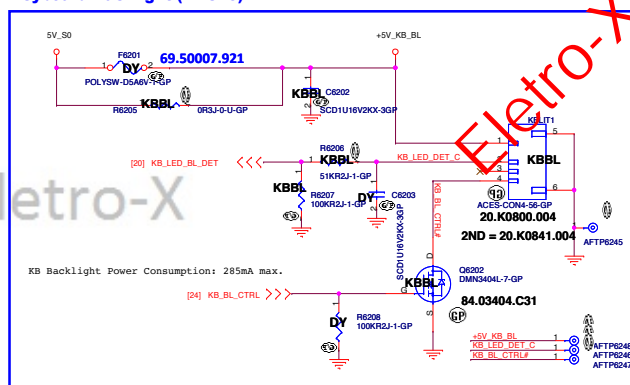
### PS2 I2C



### SMBUS

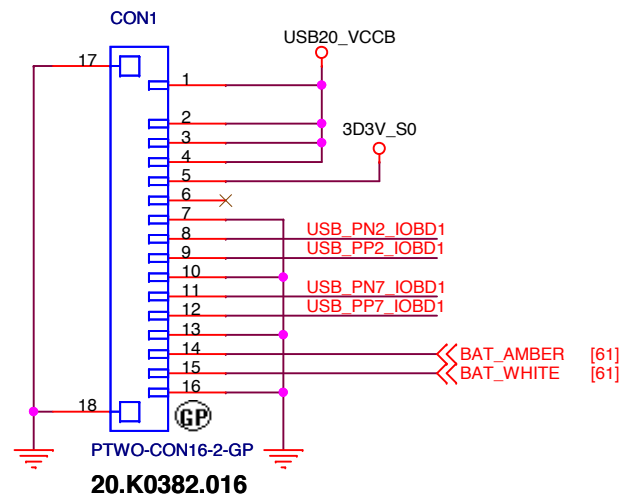


### Keyboard Backlight (DVC70)

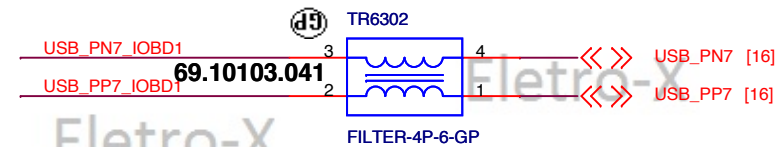
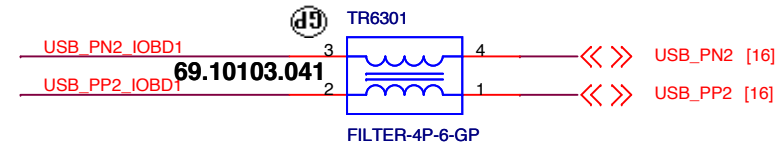


KB Backlight Power Consumption: 285mA max.

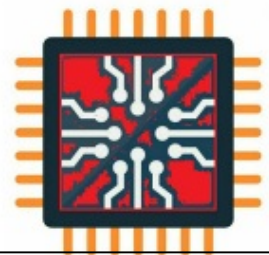
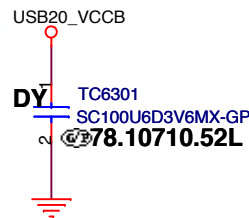
20.K0800.004  
2nd = 20.K0841.004  
3rd = 20.K0841.004



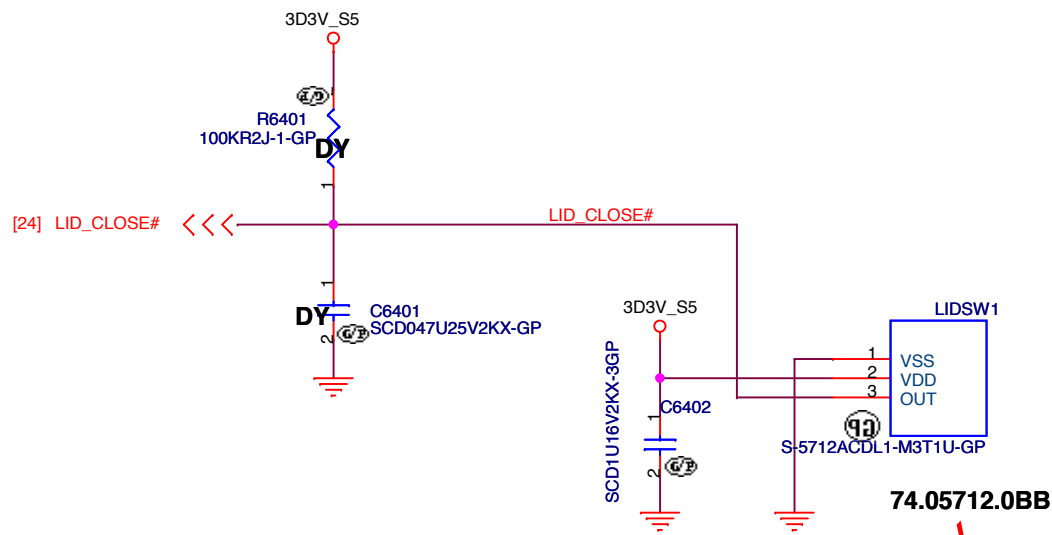
## USB2.0 Port3 Card Reader LED



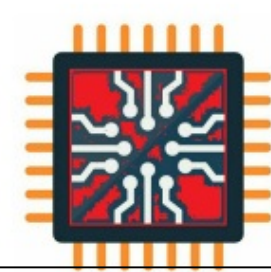
The maximum range of the PMOS output current in RTS5170 (Card Reader IC) is 400mA



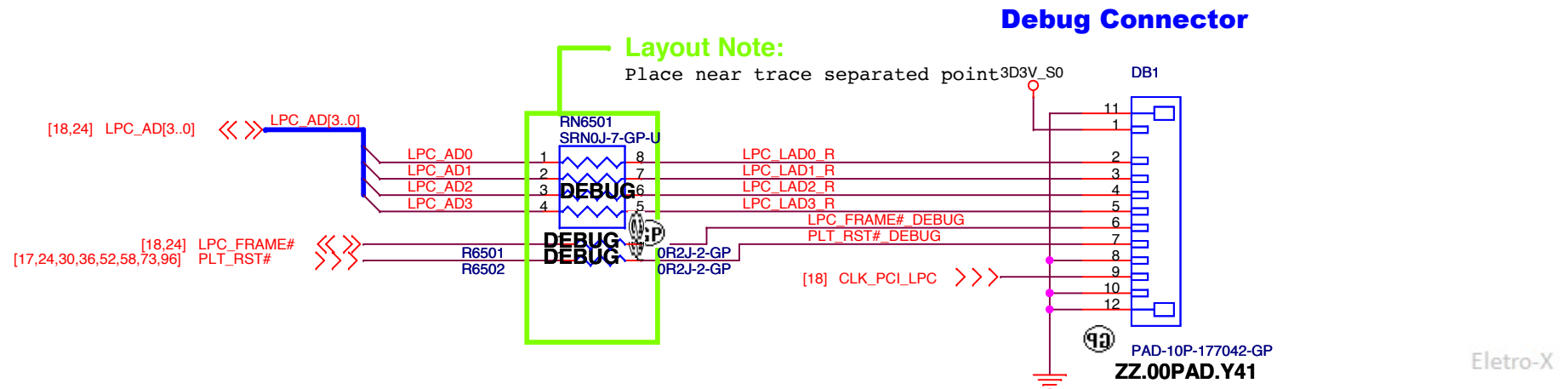
# SSID = User.Interface



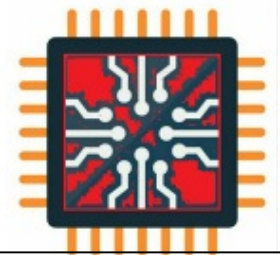
Eletro-X



# SSID = DEBUG PORT



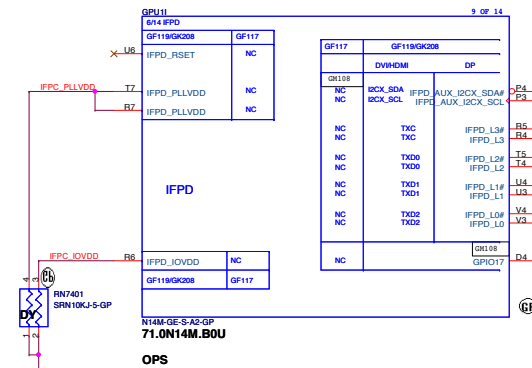
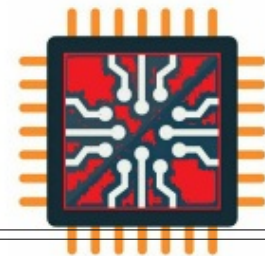
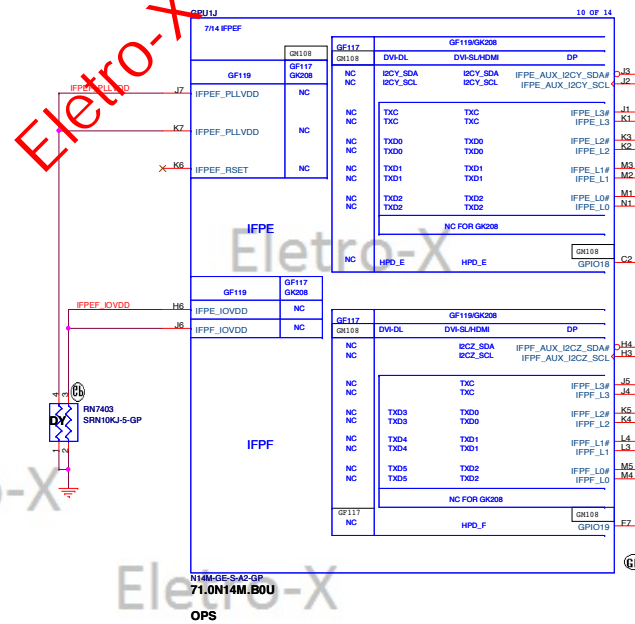
20.D0075.110: Dummy Pad with solder mask is ZZ.00PAD.Y41  
DB1 Optional: New one smaller LPC connector is 20.F1180.010.

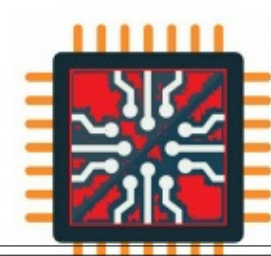






GPU1G		7 OF 14	
414 IFPB		GI108	GI118
GI118		GF117	GF118G208
GF118G208	GF117	NC	IFPA, TXC4 IFPA, TXC
IFPB, RSET	NC	NC	IFPA, TXD0F IFPA, TXD0
IFPB, PLLVDD	NC	NC	IFPA, TXD1F IFPA, TXD1
IFPB, PLLVDD	NC	NC	IFPA, TXD2F IFPA, TXD2
		NC	IFPA, TXD3F IFPA, TXD3
		NC	IFPB, TXC4 IFPB, TXC
IFPB, IOVDD	NC	NC	IFPB, TXD4F IFPB, TXD4
IFPB, IOVDD	NC	NC	IFPB, TXD5F IFPB, TXD5
		NC	IFPB, TXD6F IFPB, TXD6
		NC	IFPB, TXD7F IFPB, TXD7
		NC	
		GI118	GI118
		GI114	GI114

[illegible]



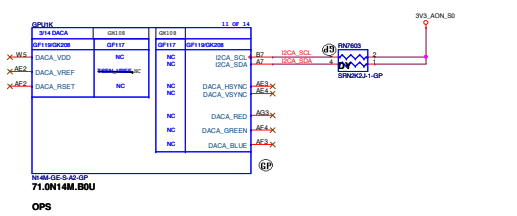


Table 3-32. GB2B-64 and GB4B-128 PLLVDD Filtering

GPU Package	PLL Rail	Capacitor Type	Footprint	Population	Location
GB2B-64 and GB4B-128	PLLVDD	0.1 µF X7R	0402	1	Under GPU
		22 µF X5R	0805	1	Near GPU
		Bead Type			
		30 Ω (ESR=0.05)	0402	1	Near GPU

Table 3-33. SP\_PLLVDD and VID\_PLLVDD Power Rail Filtering Combined

GPU Package	PLL Rails	Capacitor Type	Footprint	Population	Location
GB2B-64	SP_PLLVDD + VID_PLLVDD	0.1 µF X7R	0402	1 per ball	Under GPU
GB4B-128		4.7 µF X5R	0603	1	Near GPU
GB3-256		22 µF X5R	0805	1	Near GPU
		Bead Type			
		180 Ω (ESR=0.2)	0603	1	Near GPU

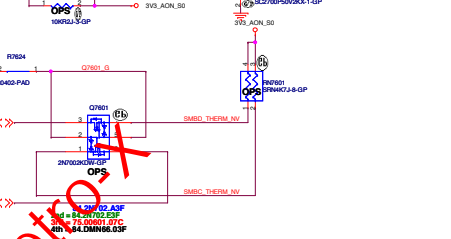
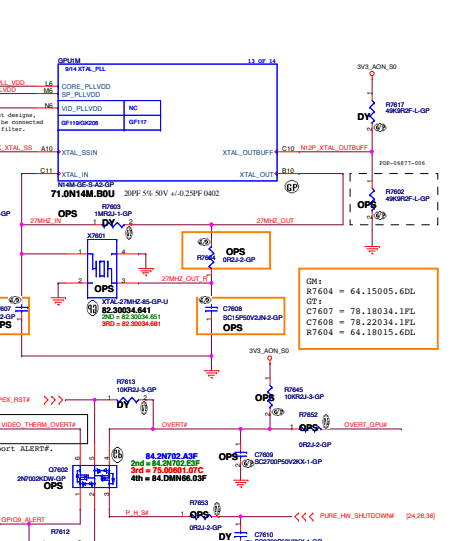
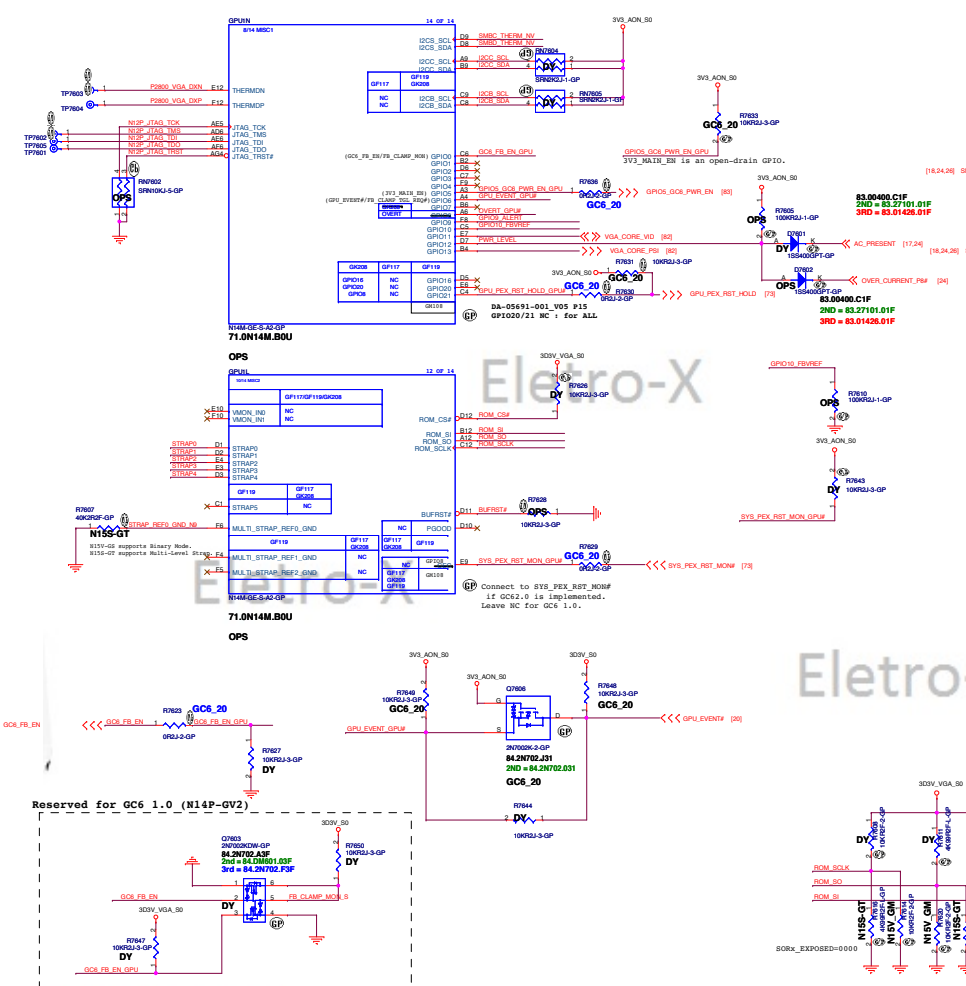
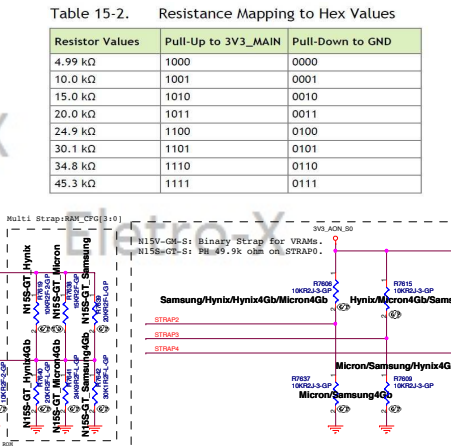


Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111



# Straps

Table 9. N15V-GM Binary Strap Mode Mapping

Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10kΩ	Pull-down to GND
ROM_SI	SUB_VEHODR	10kΩ	+Pull-up to 3V3 if VBIOS ROM exists +Pull-down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10kΩ	Pull-down to GND (no display)
STRAP0	RAM_CFG[0]	10kΩ	See note below
STRAP1	RAM_CFG[1]	10kΩ	See note below
STRAP2	RAM_CFG[2]	10kΩ	See note below
STRAP3	RAM_CFG[3]	10kΩ	See note below
STRAP4	PCIE_MAX_SPEED	10kΩ	Pull-down to GND

(RVL-06891-001)N15V- GM-S DDR3L Recommended Memories

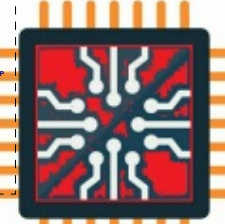
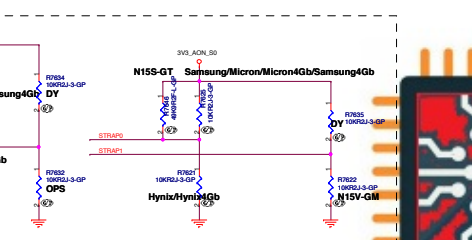
		Strap		STRAP3	STRAP2	STRAP1	STRAP0
128Mx16 DDR3L	Hynix	Ox	H5TC2G63FPR-11C	1	1	0	0
	Micron	Ox1	MT41K128M16JT-107G:K	0	0	0	1
	Samsung	Ox5	K4W2G1646E-BY11	0	1	0	1
256Mx16 DDR3L	Hynix	Ox4	H5TC4G63AFR-11C	0	1	0	0
	Micron	Ox	MT41K256M16HA-107G:E	1	1	0	1
	Samsung	Ox9	K4W4G1646D-BC1A	1	0	0	1

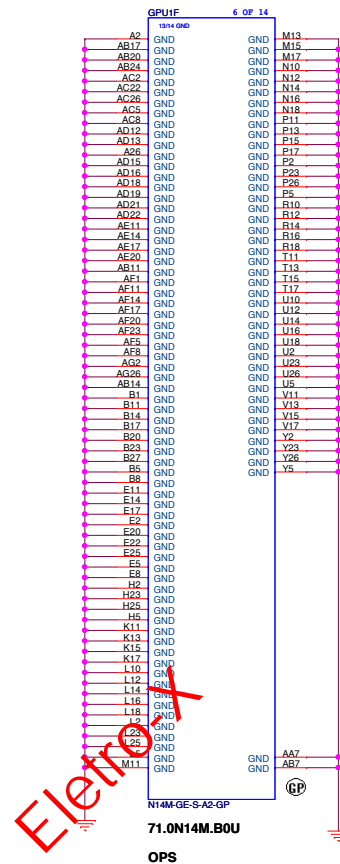
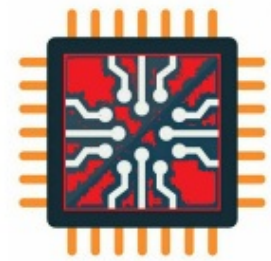
Table 10. Multi-Level Strap Differences

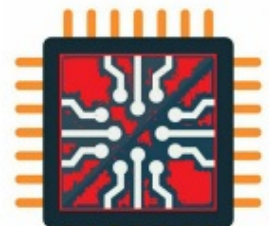
Physical Strapping Pin	GPU	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	H155-GV	PCI_DEV[4]	SUB_VEHODR	PCI_DEV[5]	PEX_PLN_EN_TERM
ROM_SI	H155-GM/-GT	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SO	H155-GM/-GT	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
STRAP0	H155-GM/-GT	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP1	H155-GM/-GT	USER[3]	USER[2]	USER[1]	USER[0]
STRAP2	H155-GM/-GT	Reserved (Keep pull-up and pull-down footprints and stuff 50kΩ pull-up)	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)
STRAP3	H155-GM/-GT	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)
STRAP4	H155-GM/-GT	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)

Table 15-2. Resistance Mapping to Hex Values

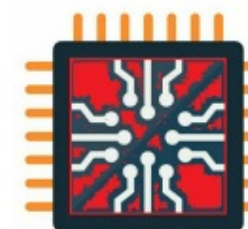
Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

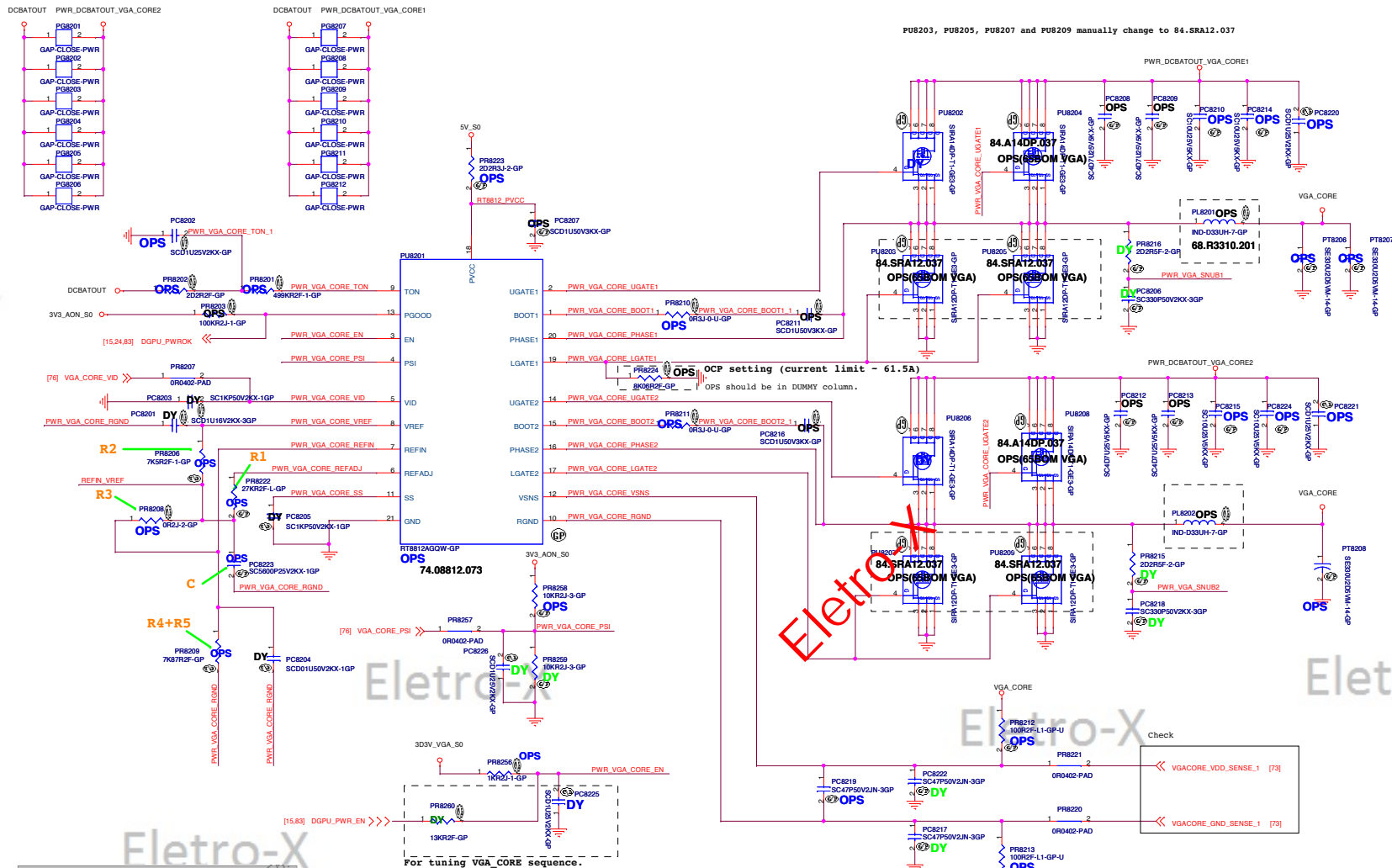


[illegible]







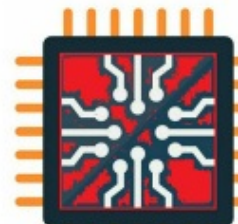


**N15V\_GM\_S  
Config D**  
Design Current=33.5A  
56.65A <OCP< 66.7A

Component	N15V-GM-S Config D	N15-S-07-S Config B
R1 (PR8222)	27K	20K
R2 (PR8206)	64.27025.60L	64.20025.60L
R3 (PR8208)	7.5K	20K
R4+R5 (PR8209)	64.75015.60L	64.20025.60L
C (PC8223)	5.6nF	2.7nF
	78.56222.2FL	78.27224.2FL

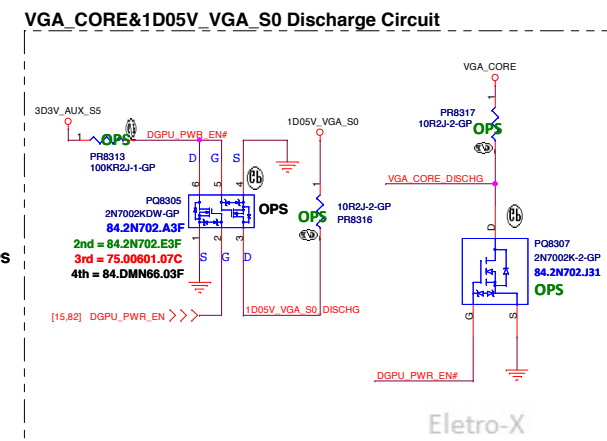
PWM-VID Specification	Config A	Config B	Config C	Config D
Vmin	0.6	0.6	0.6	0.9
Vmax	1.2	1.2	1.15	1.15
Vboot	0.875	0.9	0.9	1.025
Voltage Step Vstep	6.25	6.25	25	12.5
Number of Voltage Levels N	level 96	96	20	20
PWM Frequency F <sub>SW</sub>	MHz	1.125	0.676	0.676
PWM Minimum Pulse Width T <sub>min</sub>	μs	9.26	74	74
VID Transient Time T	<100	<100	<100	<100
Component Value				
R1 (1k)	KΩ	39	20	39
R2 (1k)	KΩ	39	20	30
R3 (1k)	KΩ	1.5	2	3
R4 (1k)	KΩ	30	18	24
R5 (1k)	KΩ	1.5	0	3
C	nF	1.5	2.7	1.8

I/P cap: 10U 25V X0805 X5R / 78.10622.51L  
Inductor: CHIP CHORE 0.22UH PCMC104T-R22 / 1mohm / Isat =60A rms / 68.R2210.10C  
O/P cap: CHIP CAP EL 330U 2.5V M6.3\*4.4 Chemi-con / 79.3371V.6CL  
H/S: SIRA14DP-T1-GE3 / 6.8mohm / 8.5mOhm 4.5Vgs / 84.A14DP.037  
L/S: SIRA06DP-T1-GE3 / 2.75mohm / 3.5mOhm 4.5Vgs / 84.SRA06.037





```
3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1D5V_VGA_S0
1D35V VGA S0 should ramp-up before 1D05V VGA S0
```



```
Cold Boot/Optimus: 3V3_AON&3V3_MAIN==>NVDD&PEX_1.05V==>FBVDD/Q
GC6 2.0 Exit: 3.3V MAIN==>NVDD&PEX1.05V
```

3V3 MAIN EN is an open-drain GPIO.

[76] GPIO5\_GC6\_PWR\_EN >>>

Could also be used for tuning sequence.

GT: R8303 = 0 ohm (62.R0034.1DL); C8301 = 0.01u (78.10324.2FL)

## Eleto-X

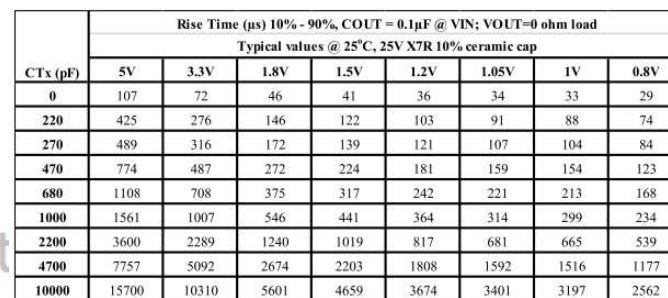
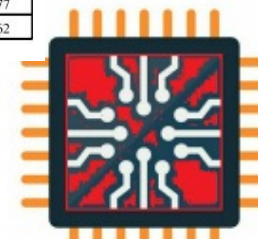
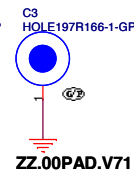
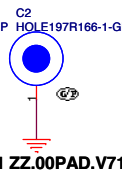
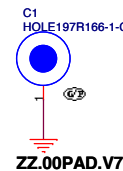
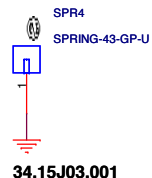
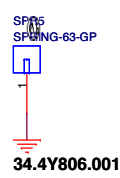
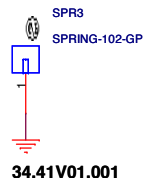
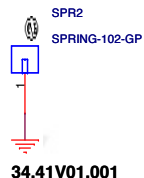
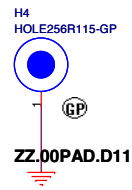
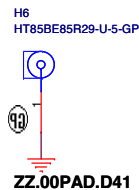
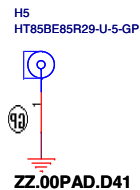
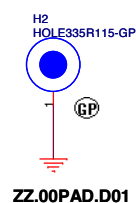
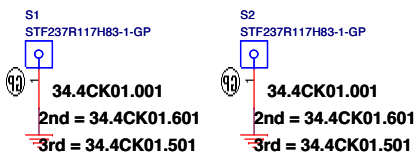


Table 1. Rise time vs. CTx value

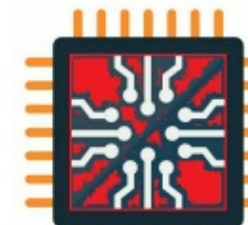
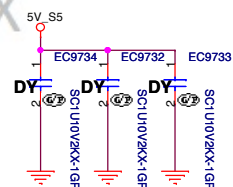
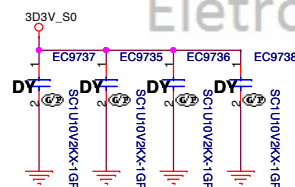
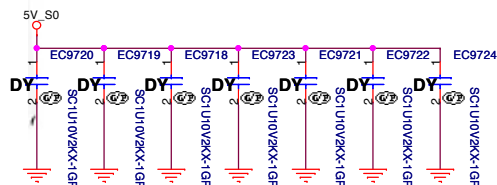
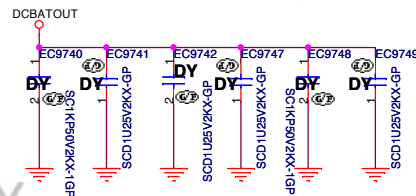
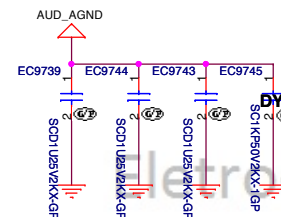
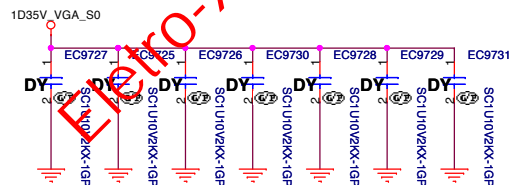
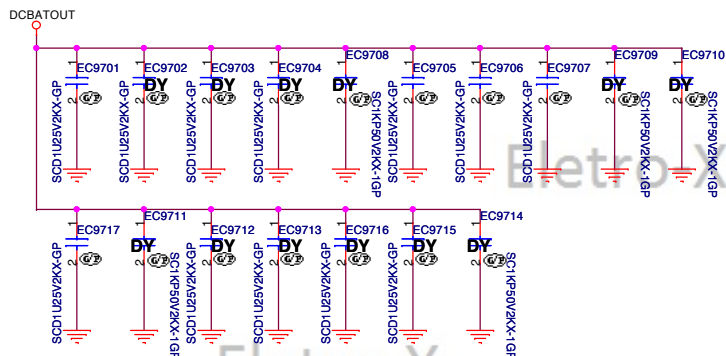


## SSID = Mechanical



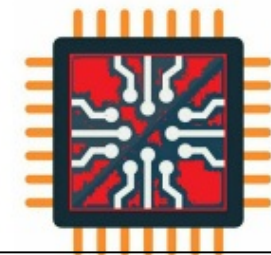
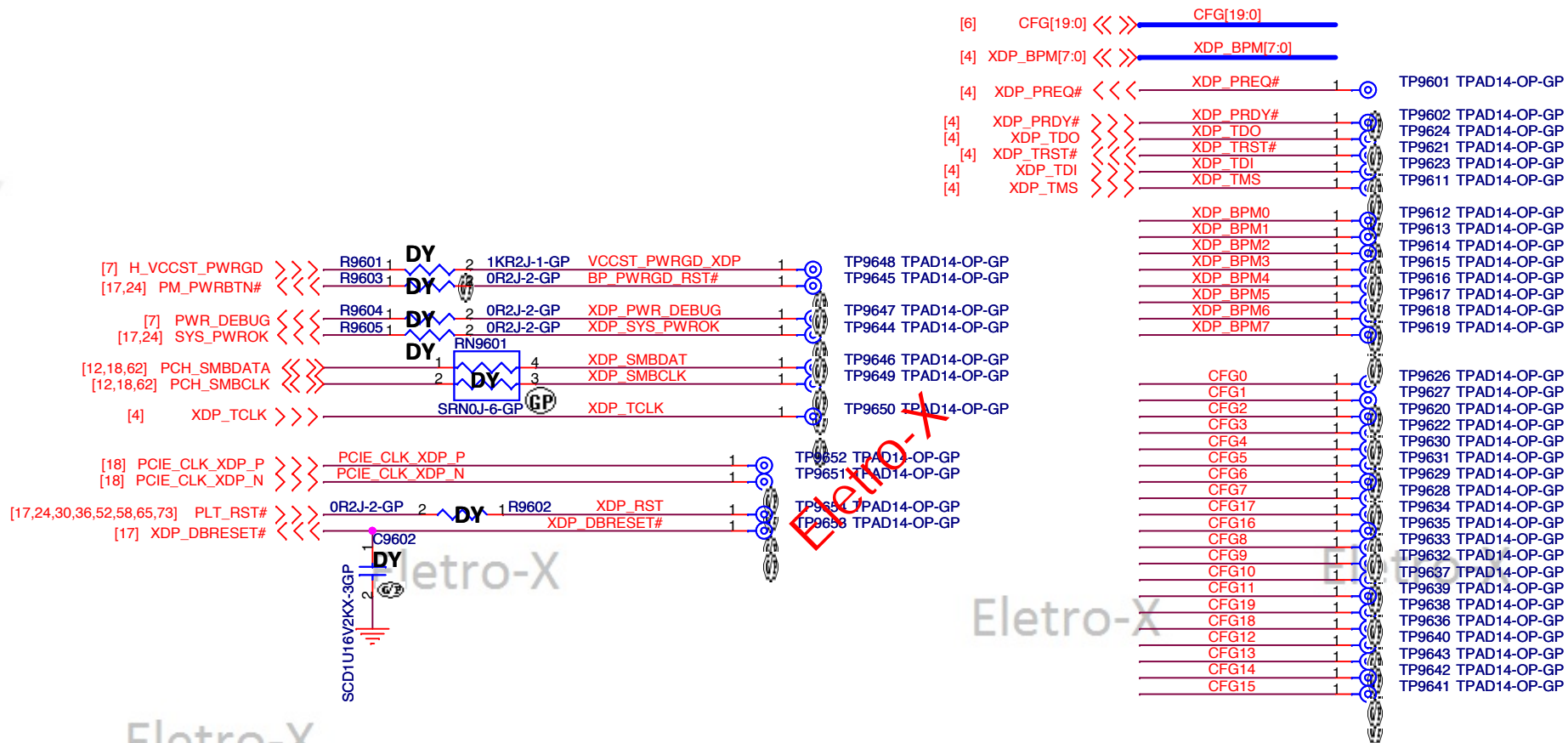
## SSID = EMI

Mind the voltage rating of the caps.

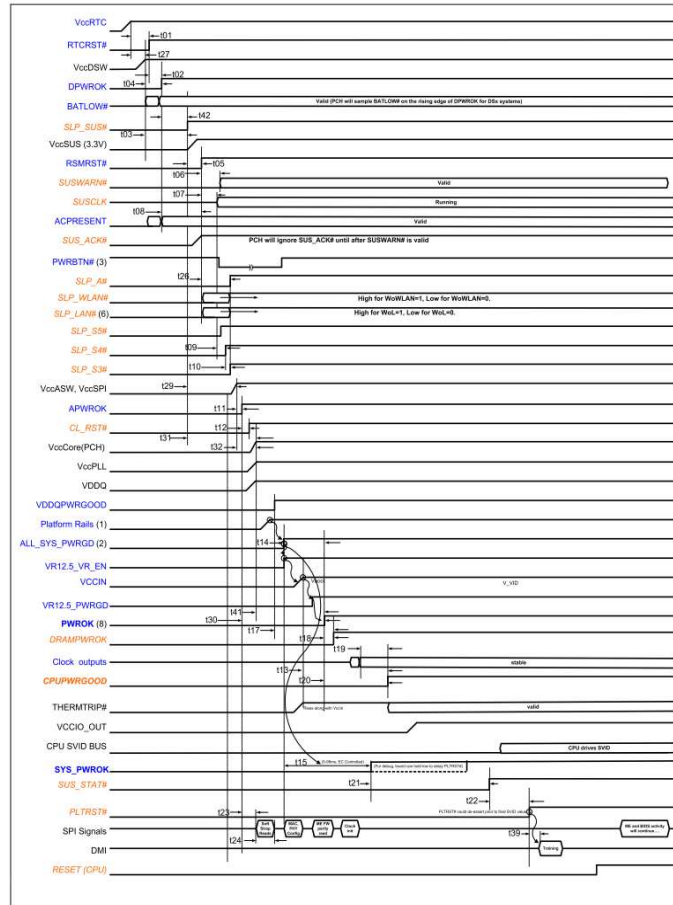


SSID = XDP

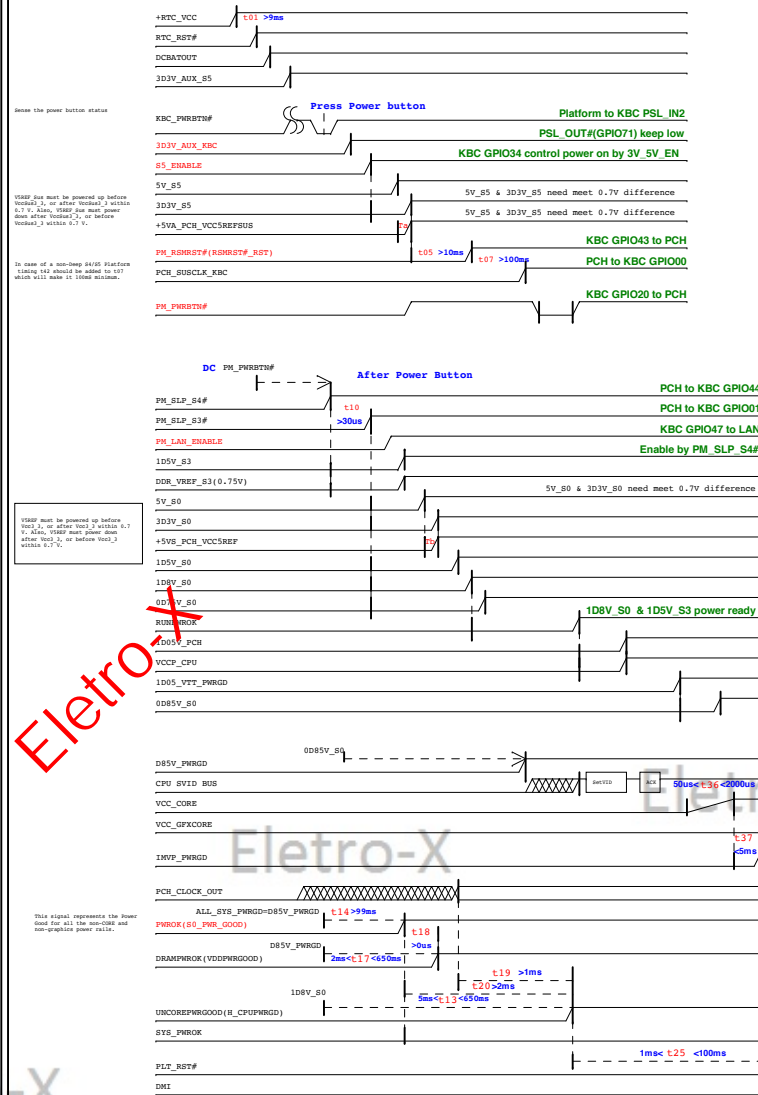
## CPU XDP



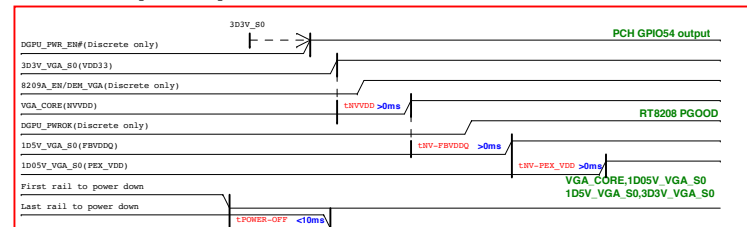
# Shark Bay Platform Power Sequence



## (DC mode)

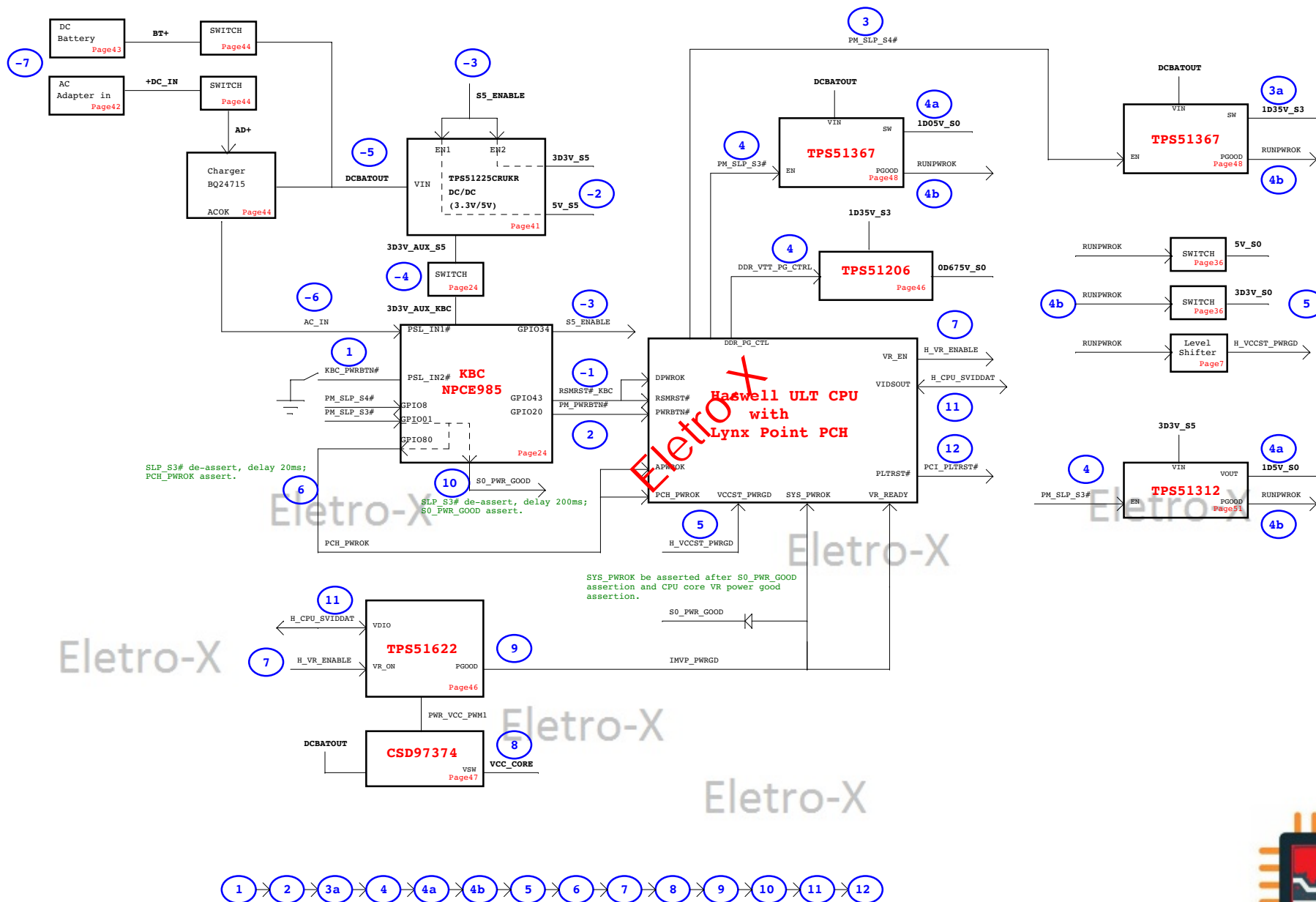


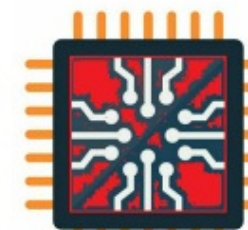
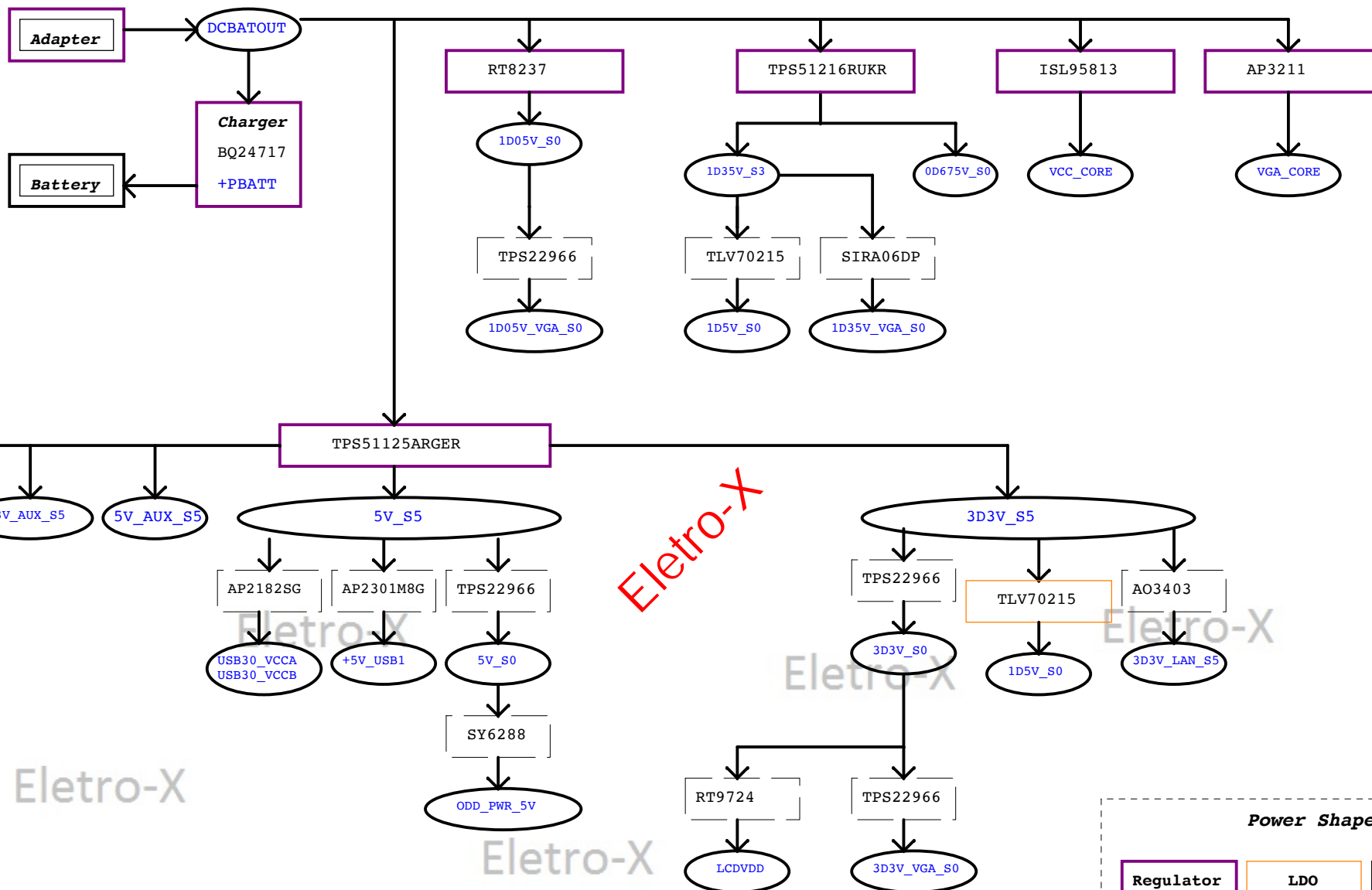
## N14P-GT Power-Up/Down Sequence



For power down, reversing the ramp-up sequence is recommended.

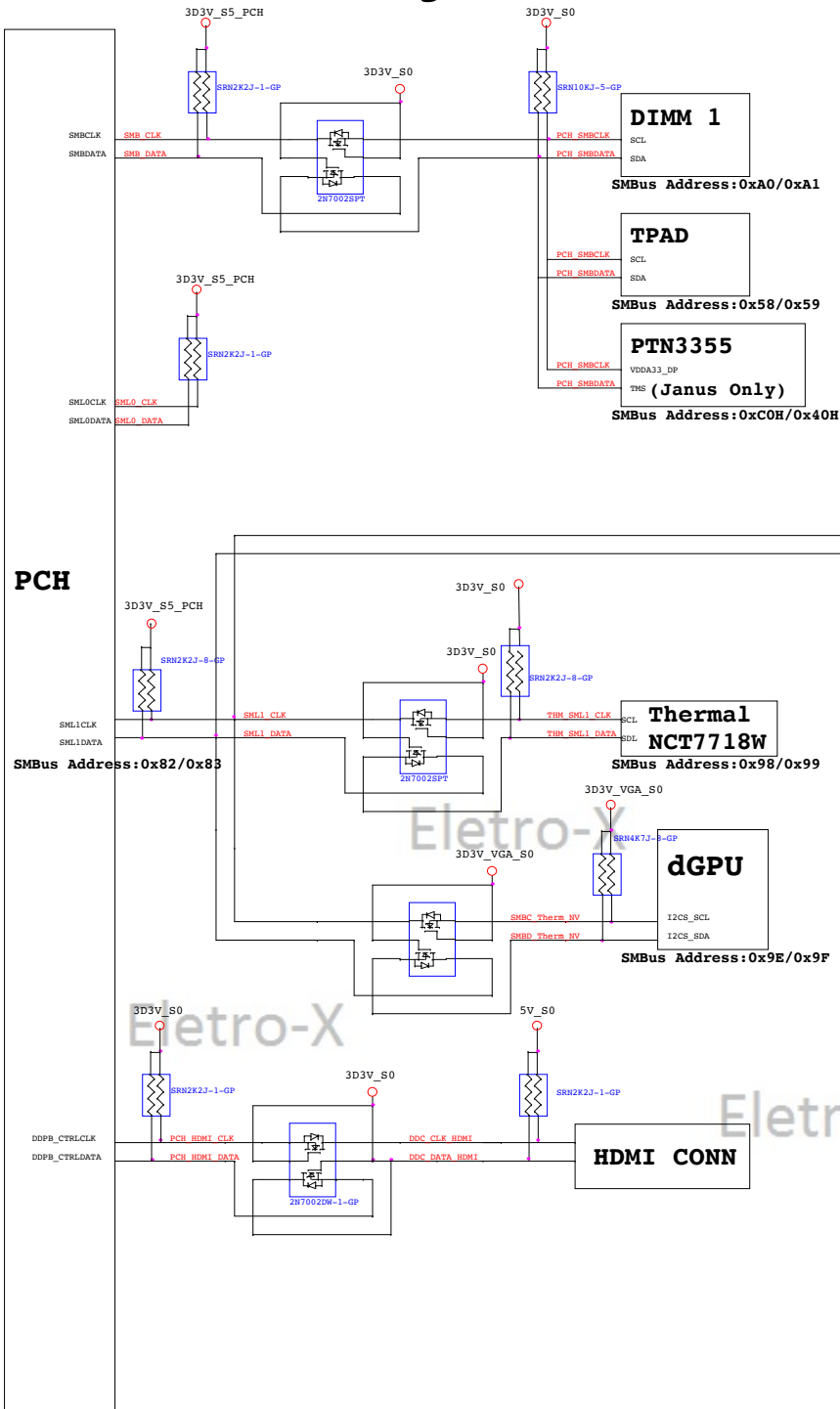
# Wistron SHARK BAY POWER UP SEQUENCE DIAGRAM



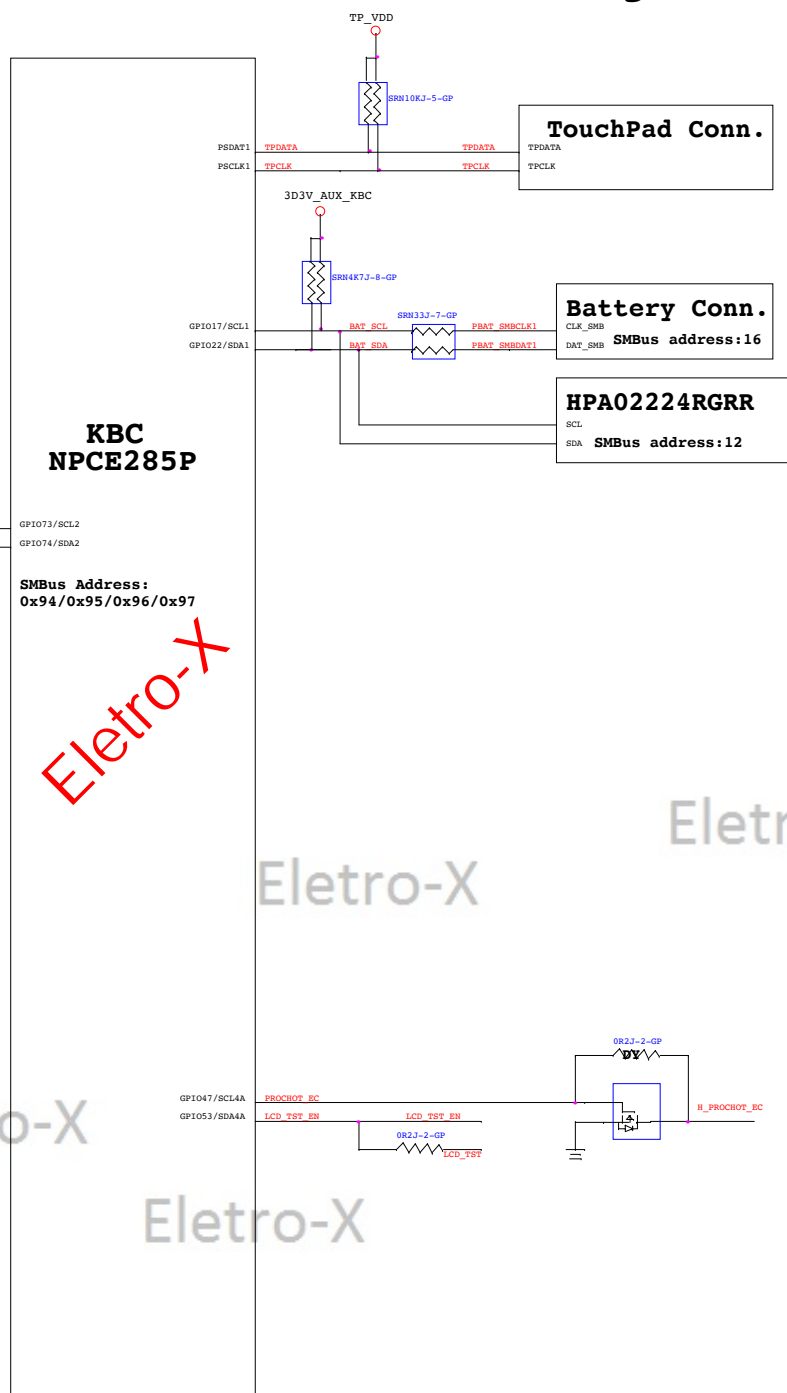




# PCH SMBus Block Diagram



# KBC SMBus Block Diagram



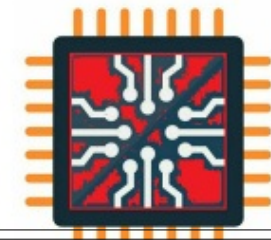
Eletro-X

Eletro-X

Eletro-X

Eletro-X

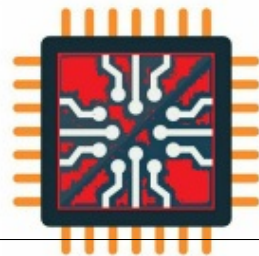
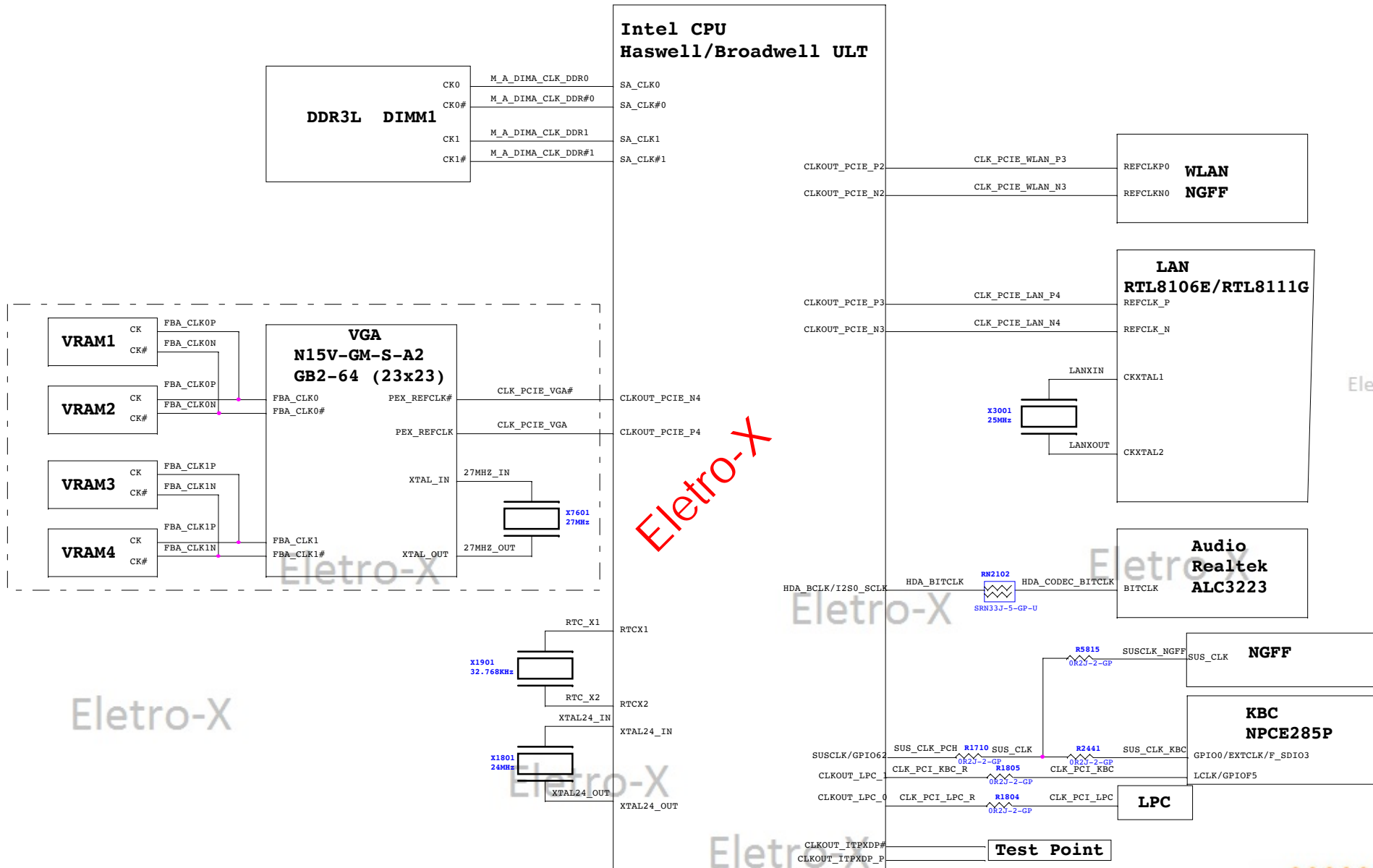
Eletro-X



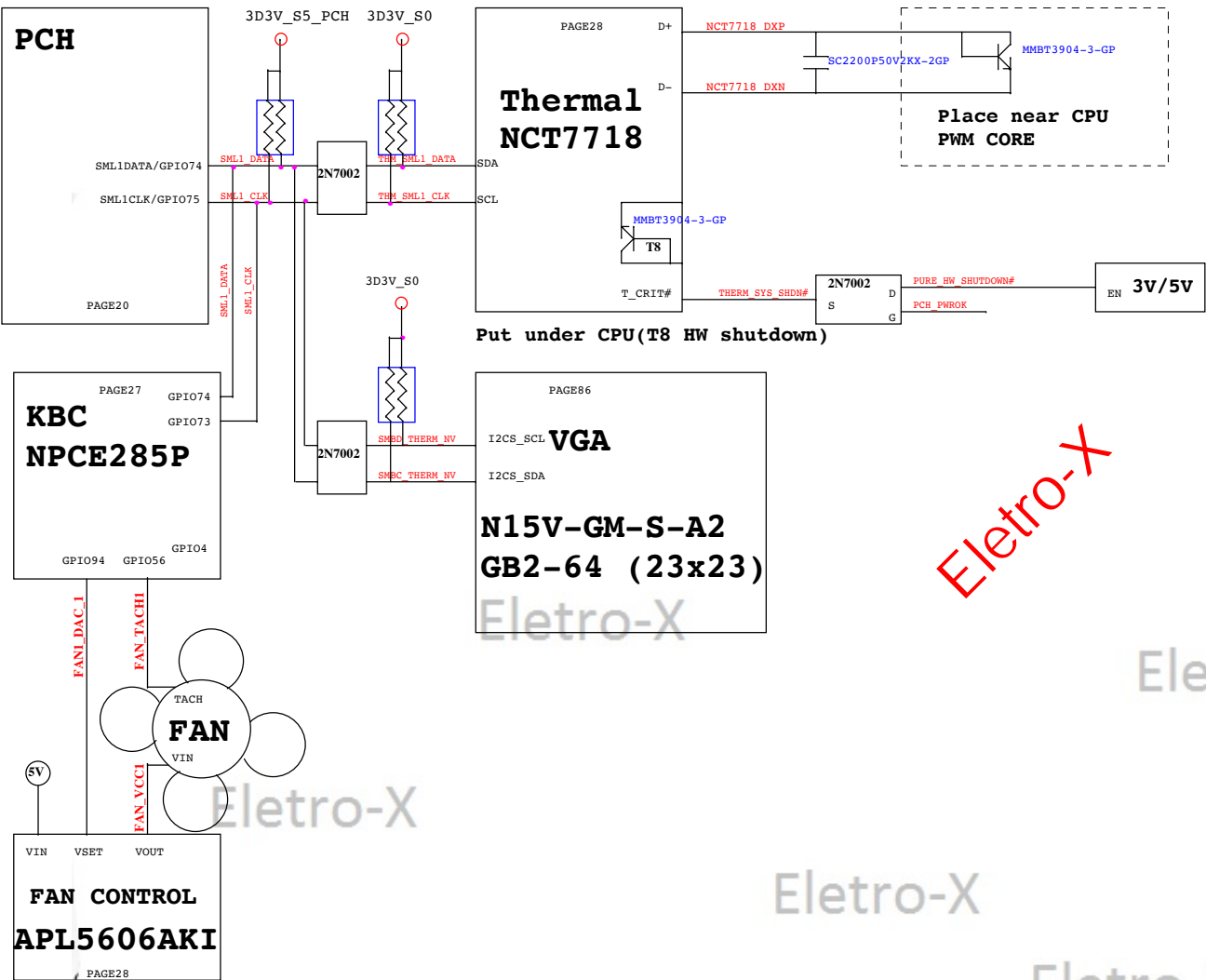
Team Eletro-X



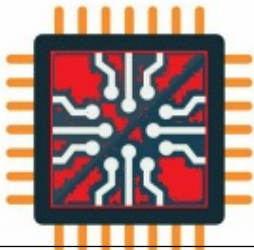
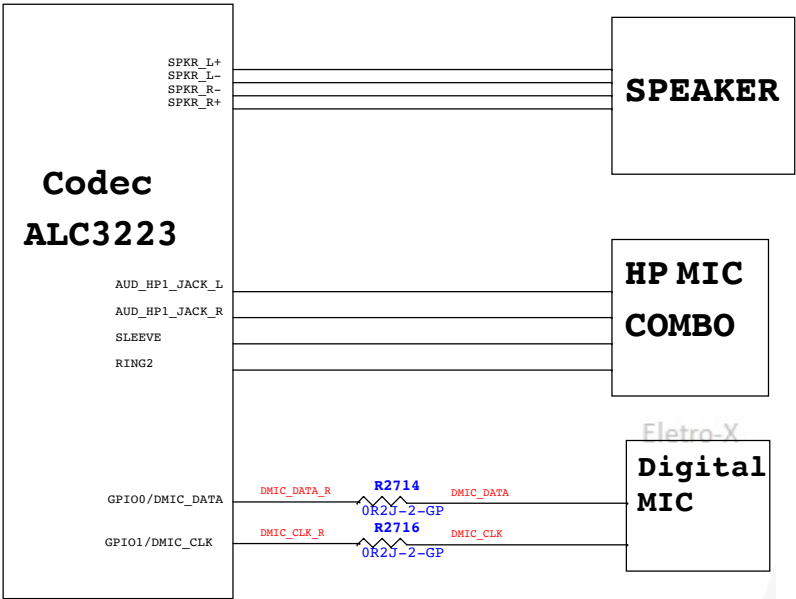
# CLK Block Diagram




# Thermal Block Diagram



# Audio Block Diagram



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Team Elsie-X